FIG. 1

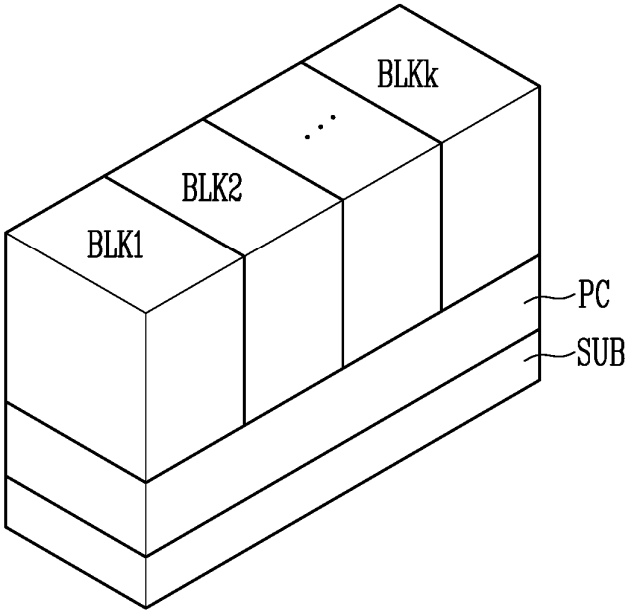


FIG. 2

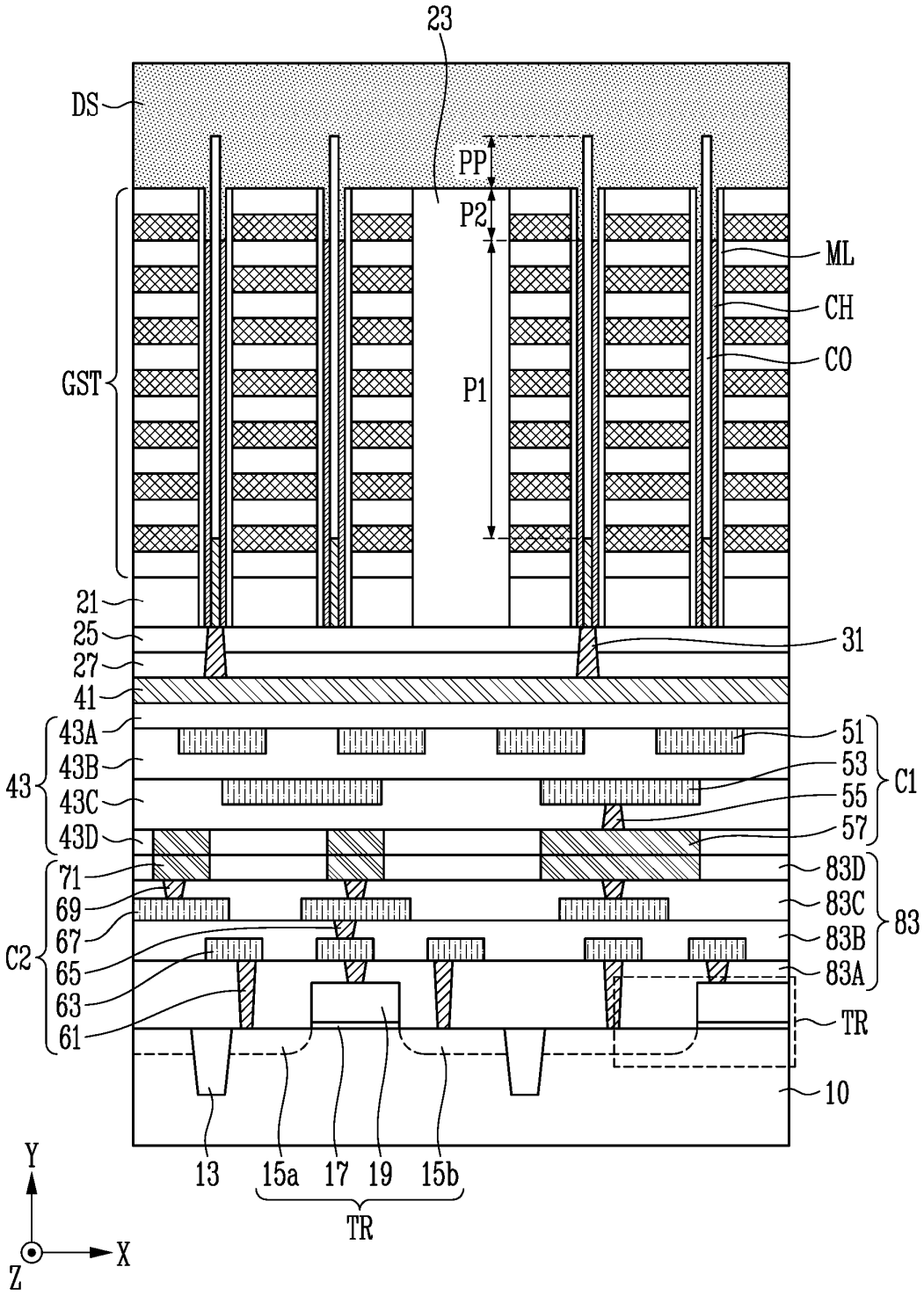

23
DS
PP
P2
ML
CH
CO
GST
P1
21
25
27
31
41
43A
43B
43
43C
43D
51
53
55
57
C1
71
69
67
65
63
61
C2
83D
83C
83B
83A
83
TR
10
13
15a
17
19
15b
TR
Y
X
Z

FIG. 3

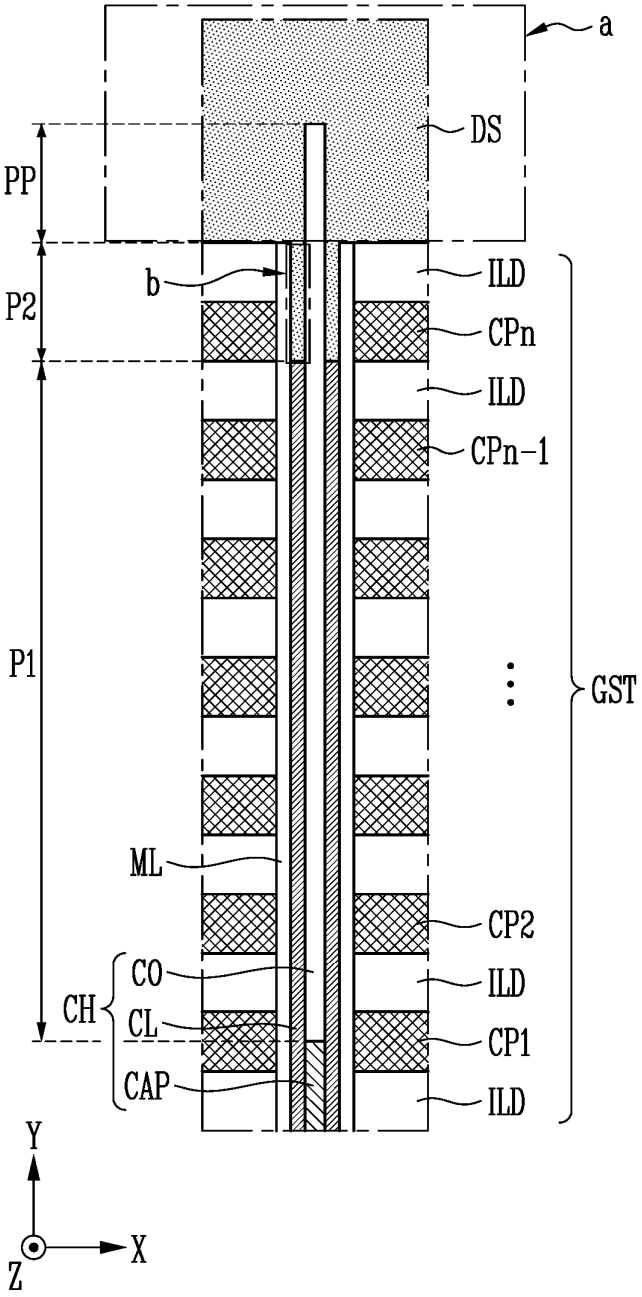

a
DS
PP
P2
b
ILD
CPn
ILD
CPn-1
P1
GST
ML
CP2
CO
ILD
CH
CL
CP1
CAP
ILD
Y
X
Z

FIG. 4A

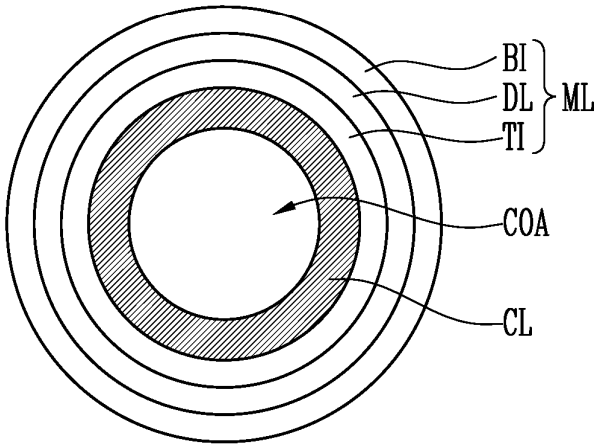


FIG. 4B

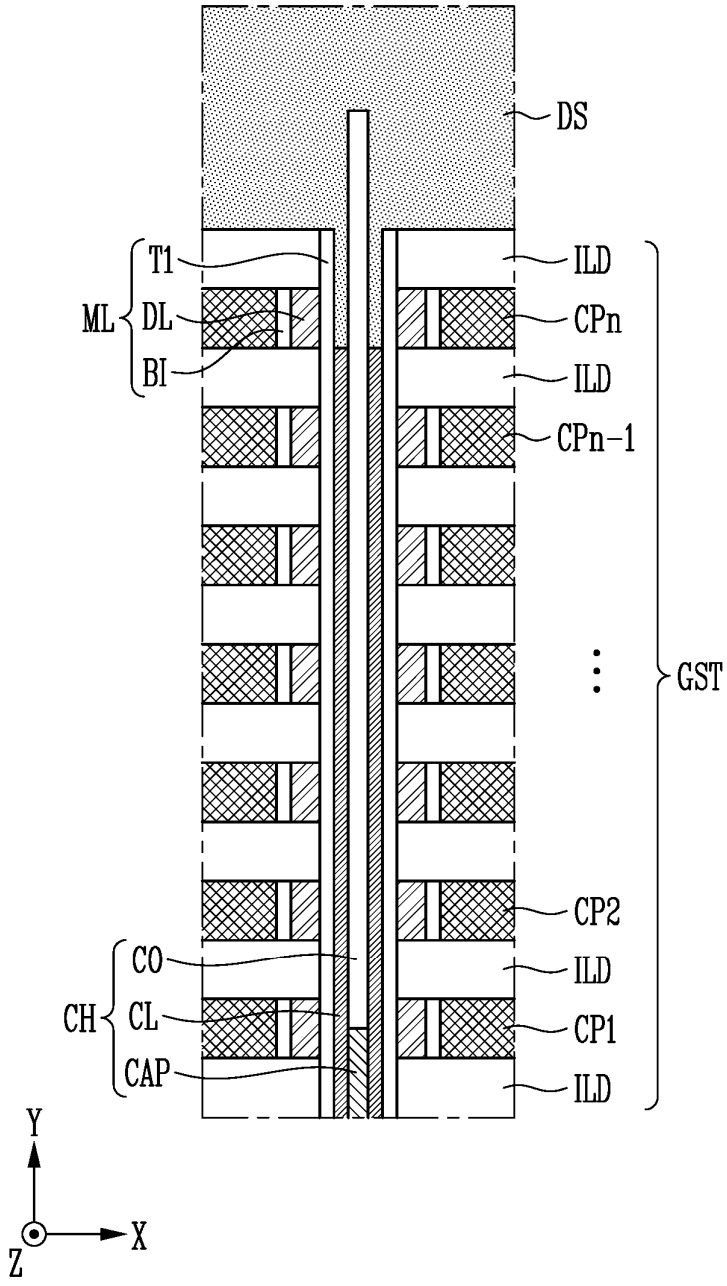

DS
T1
ML
DL
BI
ILD
CPn
ILD
CPn-1
GST
CP2
CO
CH
CL
CAP
ILD
CP1
ILD
Y
X
Z

FIG. 5A

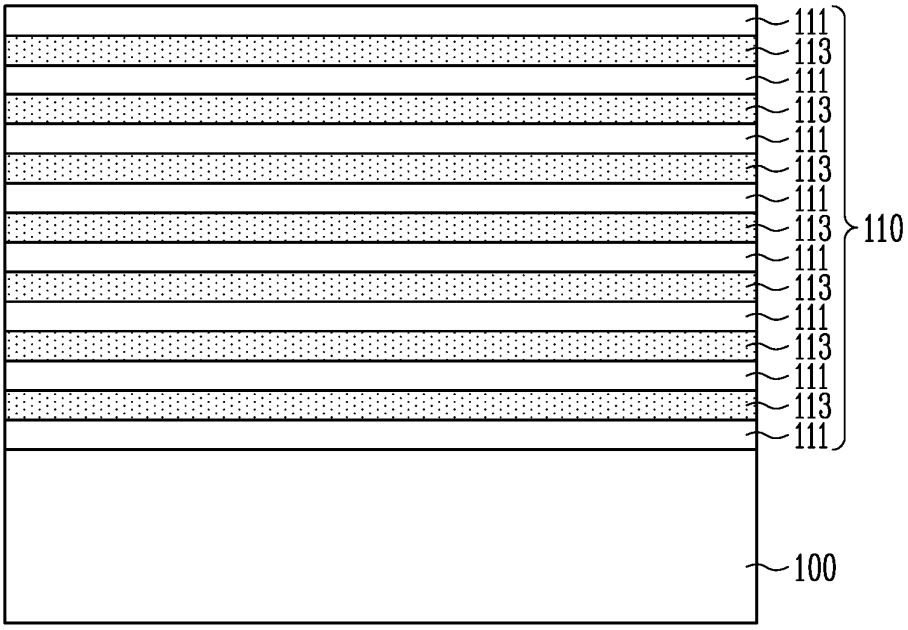

111
113
111
113
111
113
111
113
111
113
111
113
111
113
111
110
100

FIG. 5B

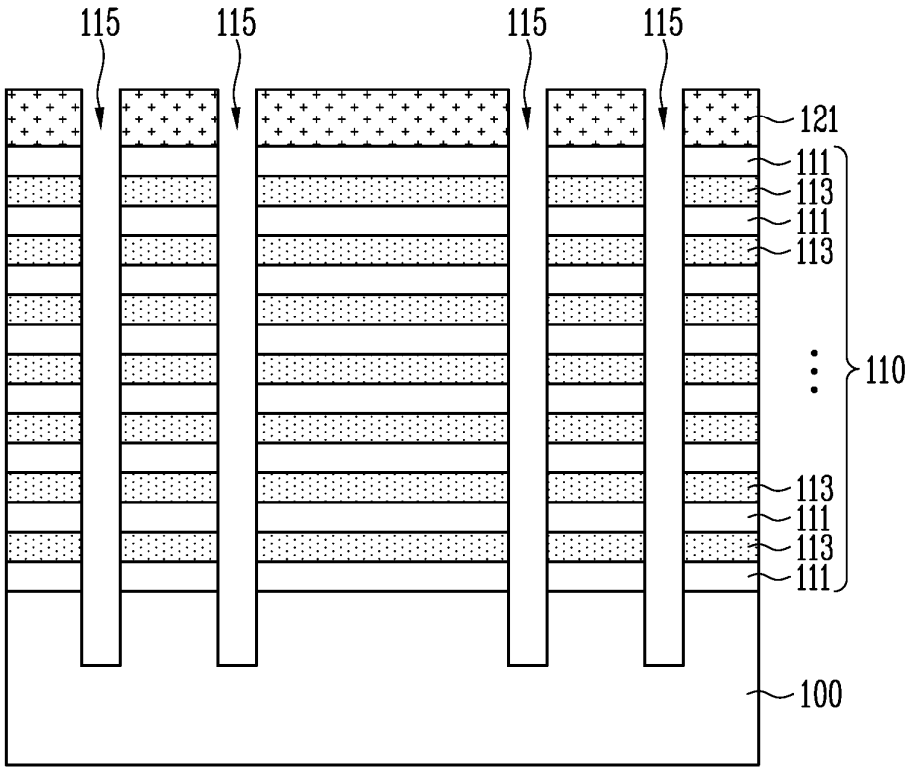


FIG. 5C

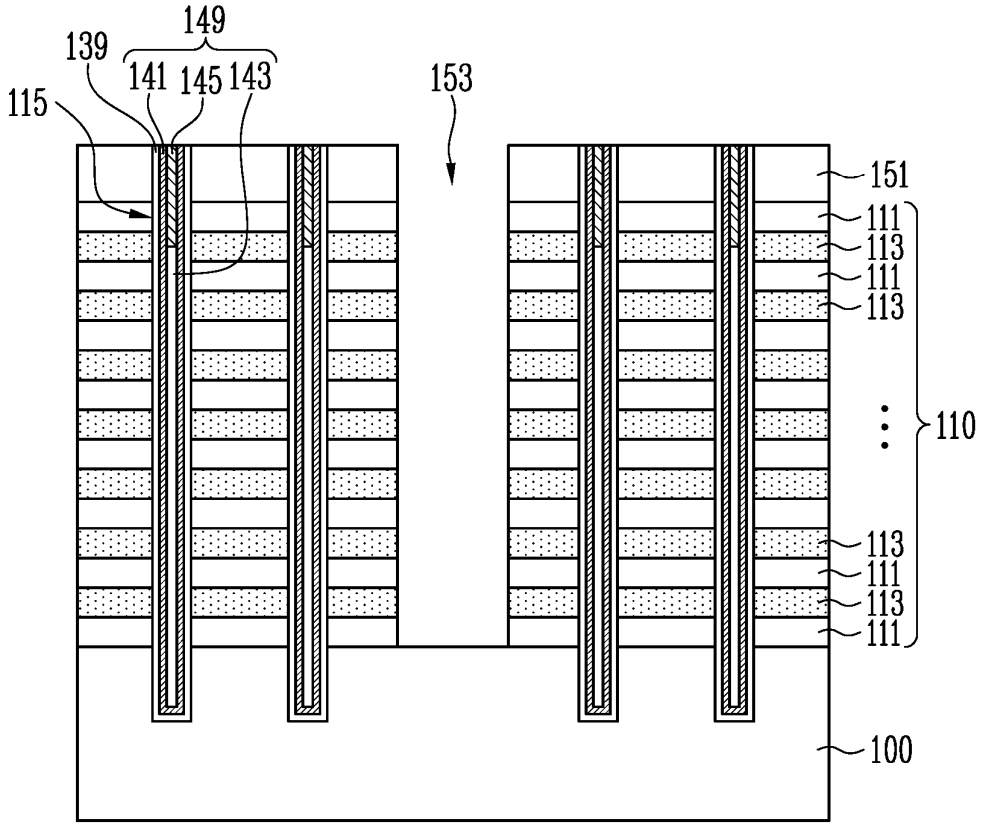

149
139
141
145
143
115
153
151
111
113
111
113
110
113
111
113
111
100

FIG. 5D

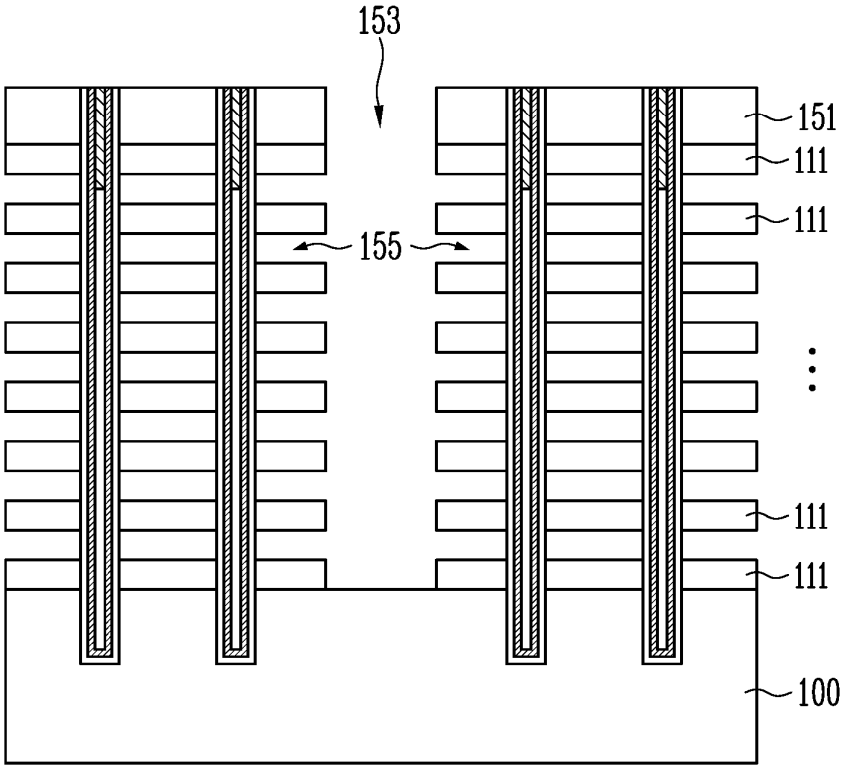


FIG. 5E

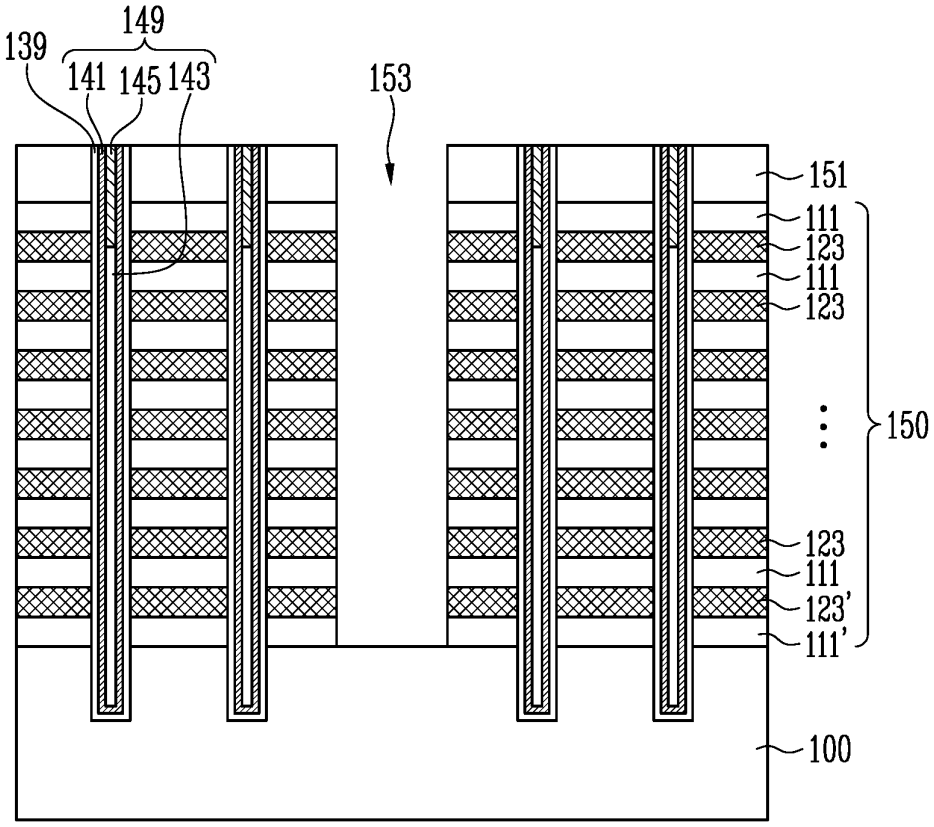

149
139
141
145
143
153
151
111
123
111
123
150
123
111
123'
111'
100

FIG. 5F

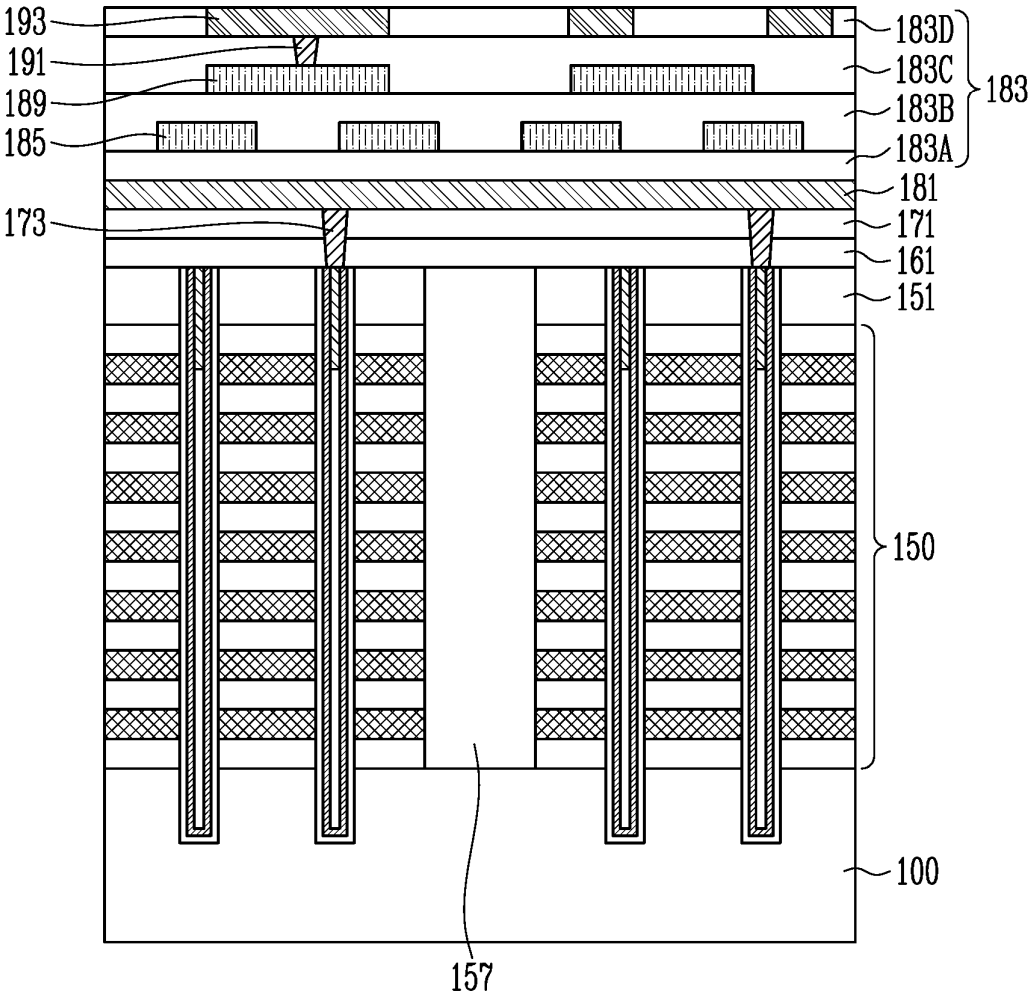

193
191
189
185
173
183D
183C
183B
183A
183
181
171
161
151
150
100
157

FIG. 6

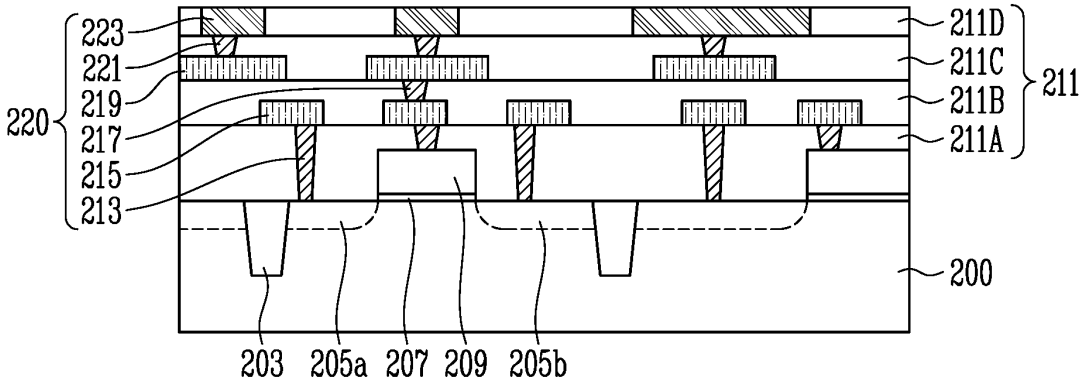

223
221
219
217
215
213
220
211D
211C
211B
211A
211
200
203
205a
207
209
205b

FIG. 7

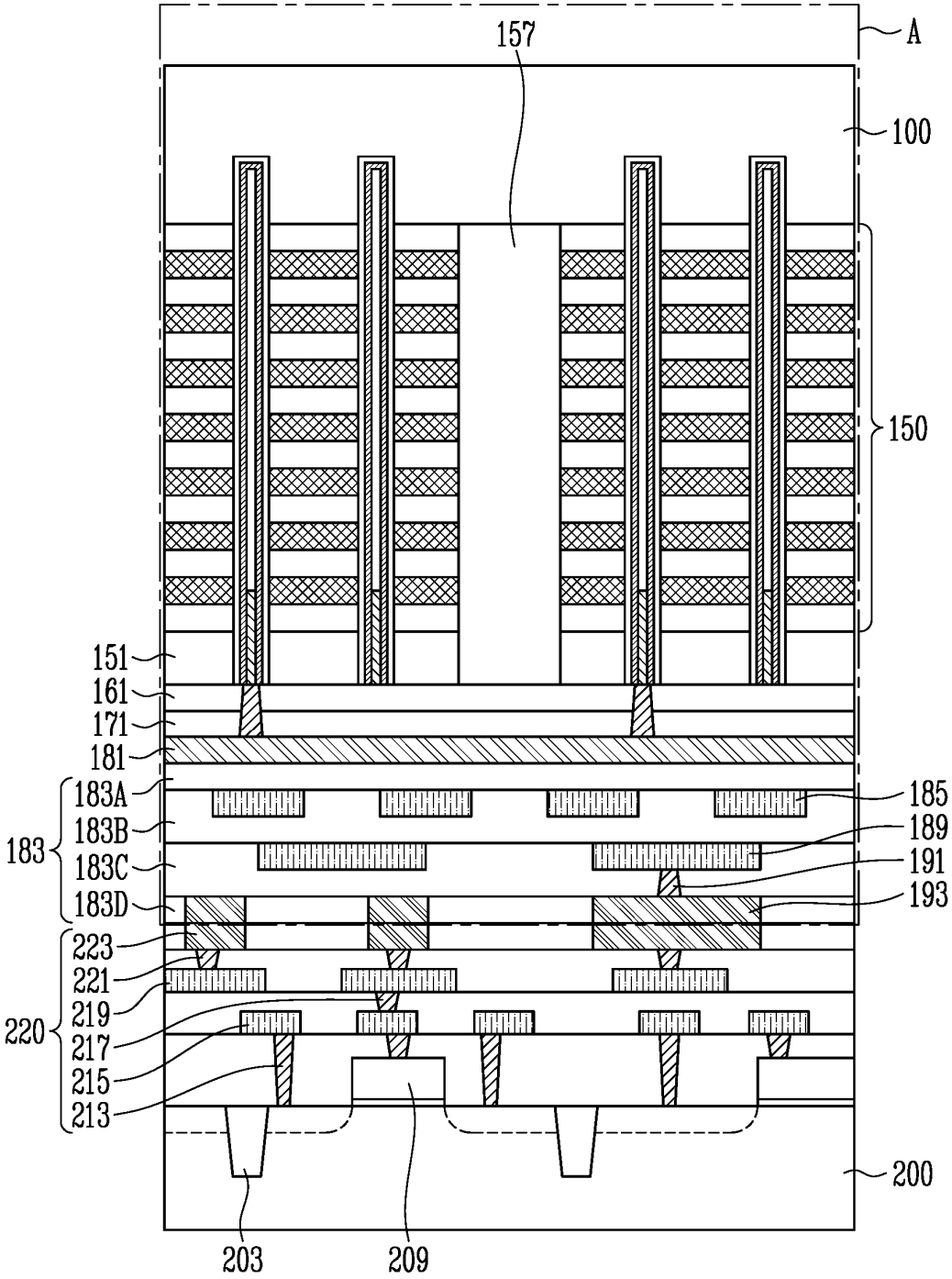

157
A
100
150
151
161
171
181
183
183A
183B
183C
183D
185
189
191
193
220
223
221
219
217
215
213
200
203
209

FIG. 8A

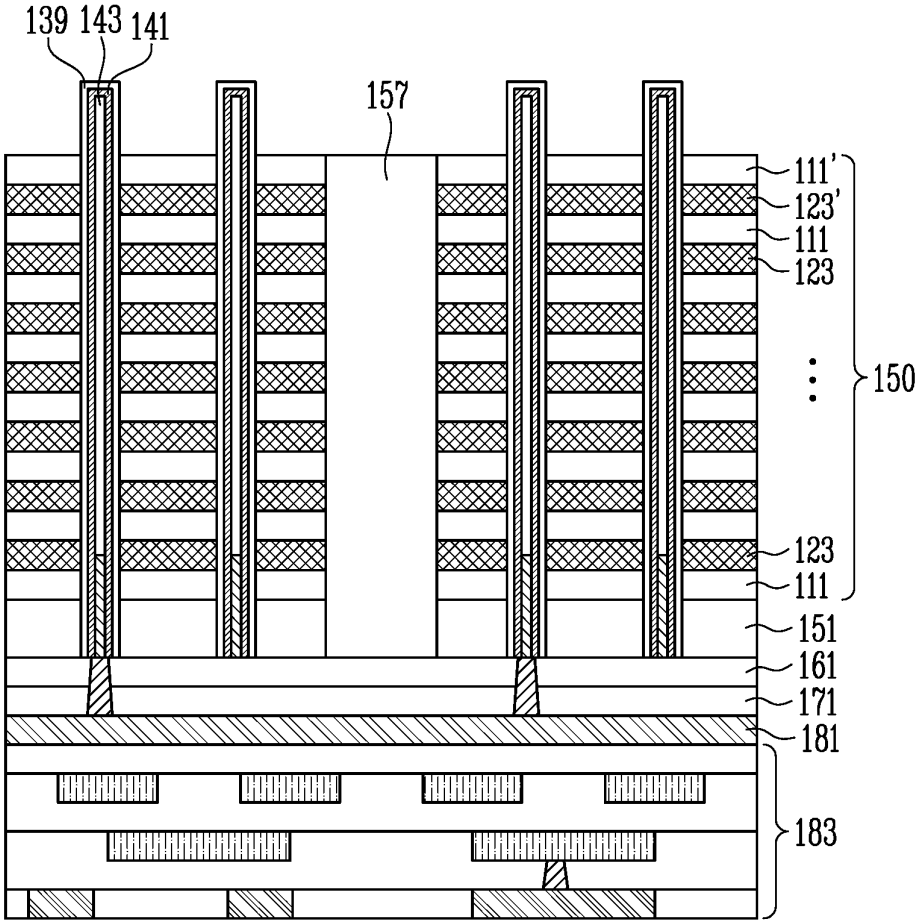


FIG. 8B

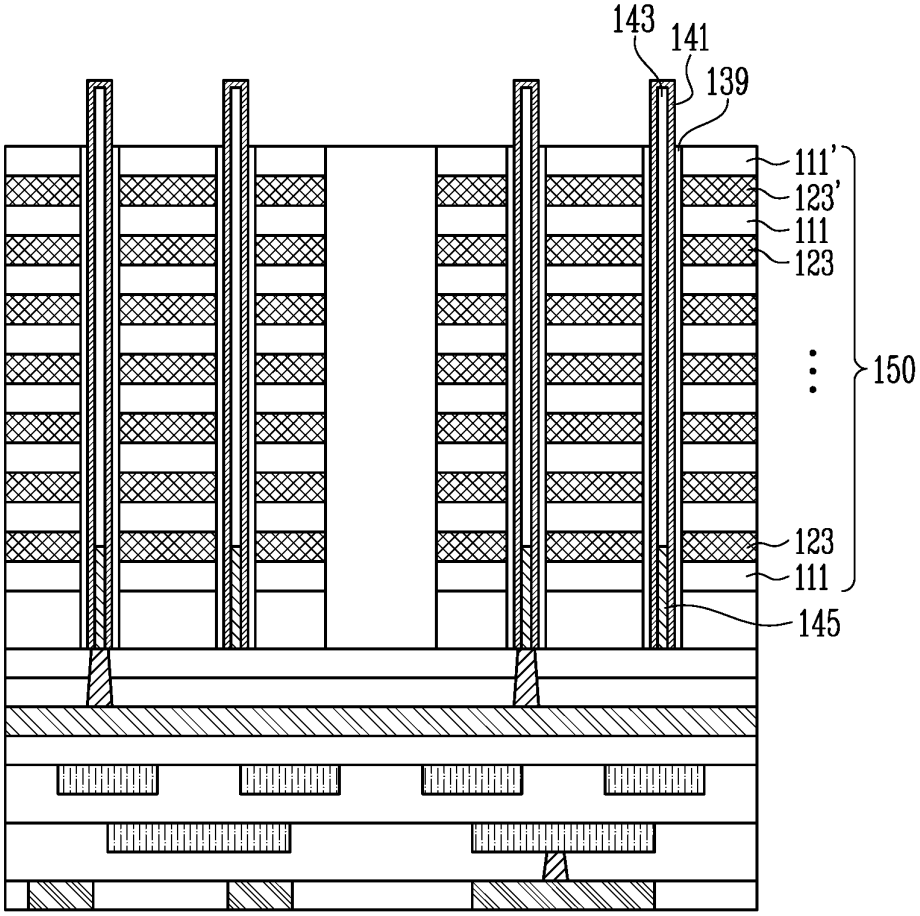


FIG. 8C

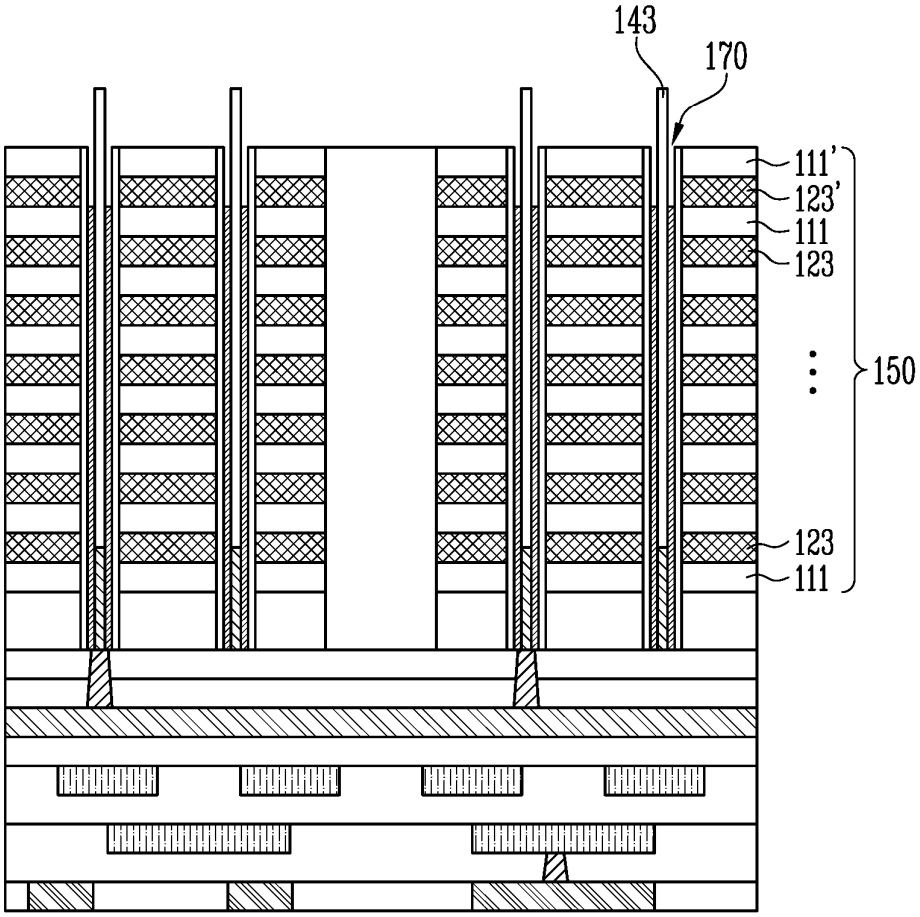


FIG. 8D

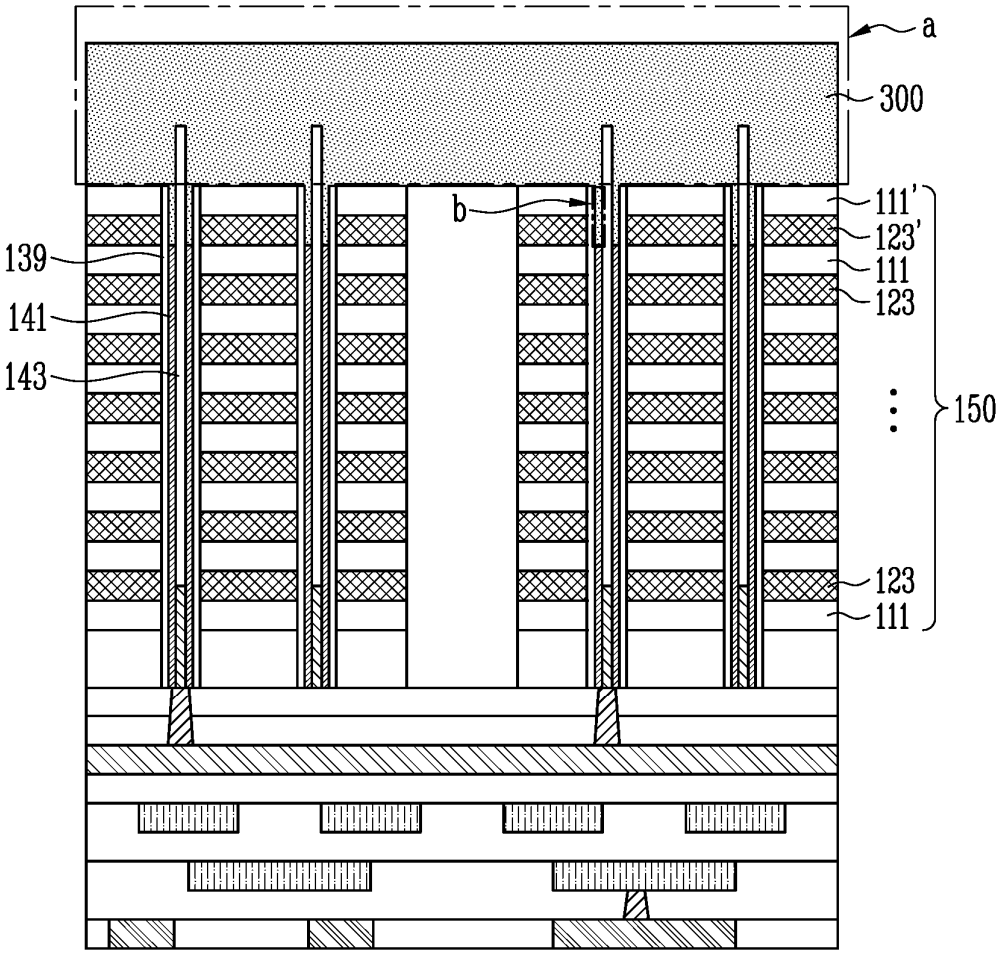


FIG. 9

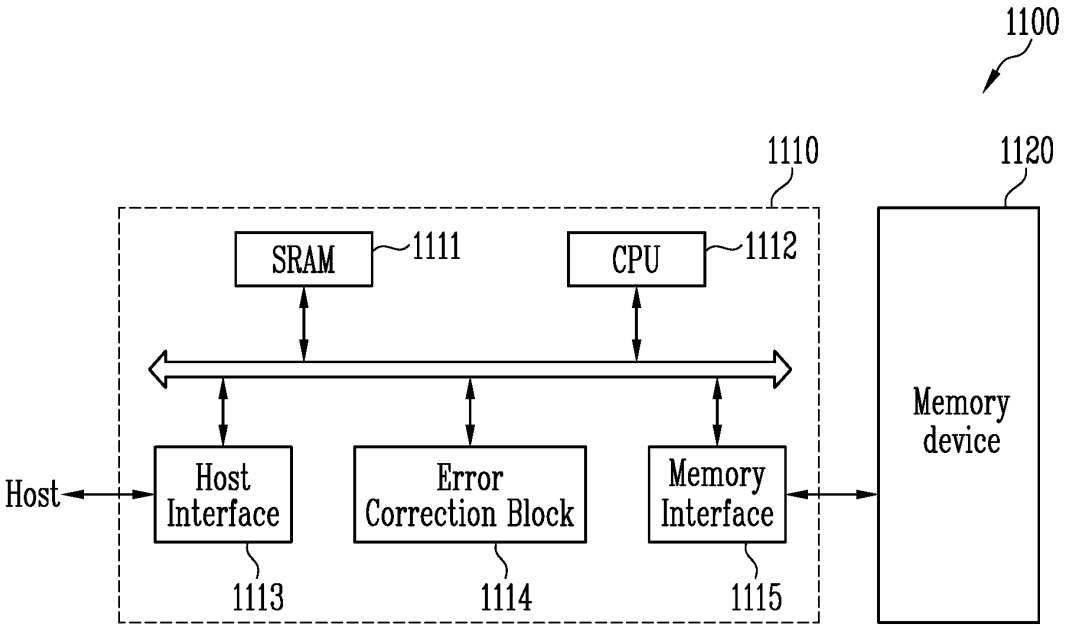
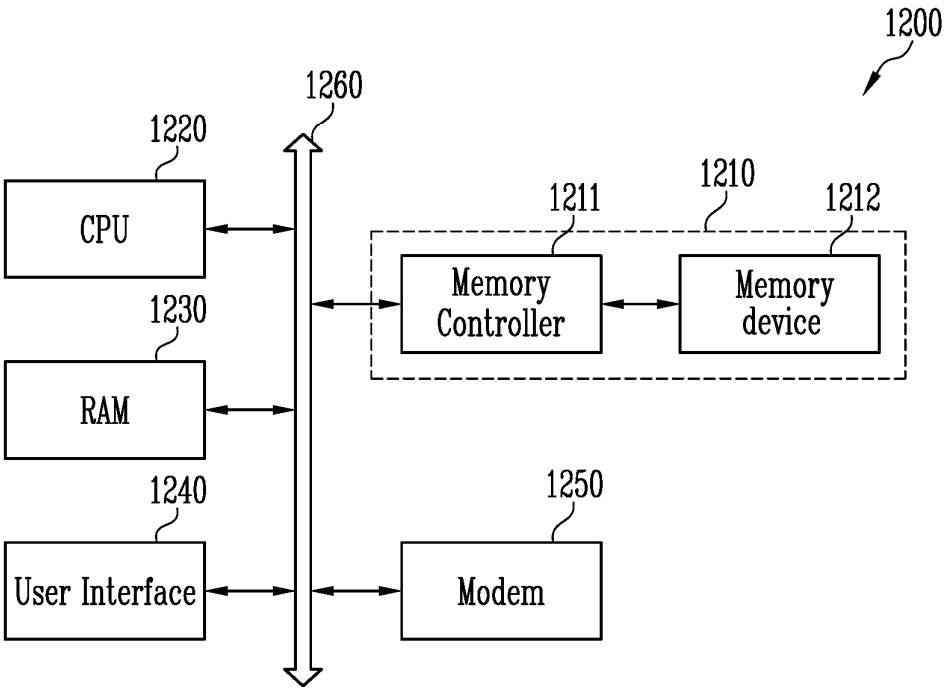

1100
1110
1120
SRAM
1111
CPU
1112
Host
Host Interface
Error Correction Block
Memory Interface
Memory device
1113
1114
1115

FIG. 10


1200
1260
1220
CPU
1230
RAM
1240
User Interface
1210
1211
1212
Memory Controller
Memory device
1250
Modem