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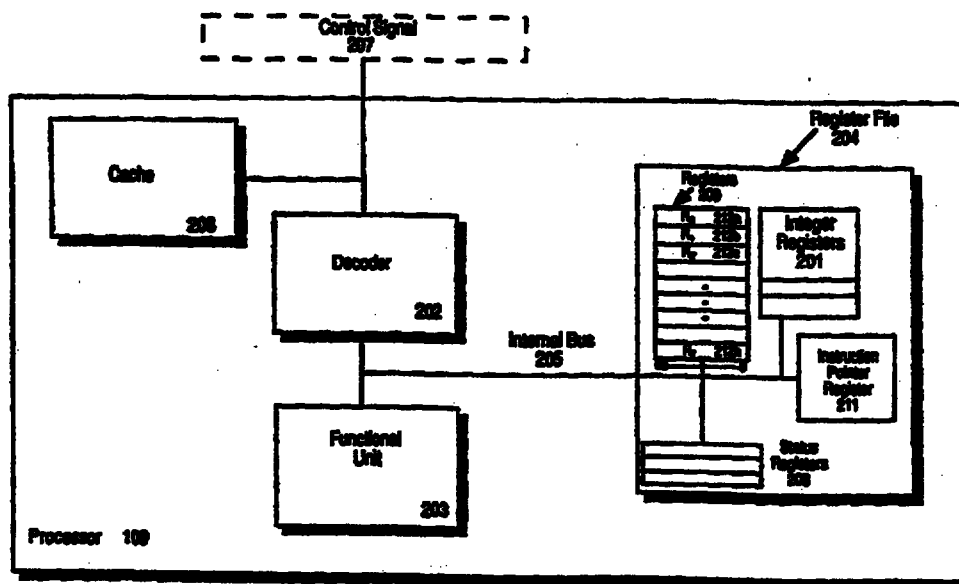
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(54) Title: MICROPROCESSOR WITH COMPARE OPERATION OF COMPOSITE OPERANDS



(57) Abstract

A processor includes a decoder (202) coupled to receive a control signal (207). The control signal has a first source address (602), a second source address (603), a destination address (605), and an operation field (601). The first source address corresponds to a first location, and the second source address corresponds to a second location. The destination address corresponds to a third location. The operation field indicates that a type of packed data compare operation is to be performed. The processor includes a circuit coupled to the decoder for comparing a first packed data being stored at the first location with a second packed data being stored at the second location and for communicating a corresponding result packed data to the third location.