performing a second etching process to remove said hard mask positioned above said first portion of said fin to thereby expose an upper surface of said first portion of said fin;

performing a third etching process to reduce a height of said first portion of said fin and thereby define a recessed upper surface of said first portion of said fin and to define a cavity within said layer of insulating material above said recessed upper surface of said first portion of said fin;

forming a second portion of said fin within said cavity on said recessed upper surface of said first portion of said fin, said second portion of said fin comprised of a second semiconducting material that is different than said first semiconducting material; and

performing a fourth etching process on said layer of insulating material such that an upper surface of said insulating material after said fourth etching process is performed is below an upper surface of said second portion of said fin.

22. A FinFET device formed by a method in accordance with any one of the preceding claims.