PACKAGE STRUCTURE AND PACKAGE COMPONENT

[0001] This application is based on and claims priority of the Chinese Patent Application No. 202411183523.4, filed with China National Intellectual Property Administration on August 26, 2024 and entitled "PACKAGE STRUCTURE AND PACKAGE COMPONENT". The above-referenced application is incorporated herein by reference in its entirety.

TECHNICAL FIELD

[0002] Embodiments of the present disclosure relate to the field of semiconductor technologies, and in particular, to a package structure and a package component.

BACKGROUND

[0003] Recently, the demands for portable apparatuses rapidly increase in the electronic product market. Therefore, an electronic component installed on an electronic product is increasingly required to be miniaturized and lightweight.

SUMMARY

[0004] According to a first aspect of the embodiments of the present disclosure, a package structure is provided and includes:

dielectric layers;

first re-distribution layers, located in the dielectric layers;

second re-distribution layers, located on the first re-distribution layers, where the first re-distribution layers are electrically connected to the second re-distribution layers, and the tops of the second re-distribution layers protrude from the dielectric layers;

chips, located on the dielectric layers; and

wires, connecting the chips to the second re-distribution layers.

[0005] According to a second aspect of the embodiments of the present disclosure, a package structure is provided and includes:

dielectric layers;

first re-distribution layers, located in the dielectric layers;

second re-distribution layers, located on the first re-distribution layers, where the first re-distribution layers are electrically connected to the second re-distribution layers, and the tops of the second re-distribution layers protrude from the dielectric layers;

chips, located on the dielectric layers; and

wires, connecting the chips to the second re-distribution layers;

wherein the dielectric layers comprising:

a first dielectric layer, located on a fourth dielectric layer;

a second dielectric layer, located on the first dielectric layer; and

a third dielectric layer, located on the second dielectric layer, a thickness of the third dielectric layer being equal to a thickness of the first dielectric layer, a thickness of the fourth dielectric layer being less than the thickness of the first dielectric layer, and the thickness of the first dielectric layer being equal to a thickness of the second dielectric layer.

[0006] According to a third aspect of the embodiments of the present disclosure, a package component is provided and includes:

a substrate; and

a package structure, where the package structure is disposed on the substrate.

[0007] In conclusion, the embodiments of the present disclosure provide the package structure and the package component. The first re-distribution layers and the second re-distribution layers are formed in the dielectric layers, the tops of the second re-distribution layers protrude from the dielectric layers, then, the chips are disposed on the dielectric layers, and the second re-distribution layers are connected to the chips through the wires. The overall thickness of the dielectric layers is relatively small, and the tops of the second re-distribution layers are outside the dielectric layers. Therefore, the wires can be directly connected to the second re-distribution layers, to implement miniaturization of the package structure.

BRIEF DESCRIPTION OF DRAWINGS

[0008] FIG. 1 is a schematic diagram of a package structure according to an example embodiment;

[0009] FIG. 2 is a schematic diagram of dielectric layers according to an example embodiment;

[0010] FIG. 3 is a schematic diagram of an intermediate conductive pattern according to an example embodiment;

[0011] FIG. 4 is a schematic diagram of a second re-distribution layer according to an example embodiment;

[0012] FIG. 5 is a schematic diagram of chip stacking according to an example embodiment;

[0013] FIG. 6 is a schematic diagram of another package structure according to an example embodiment;

[0014] FIG. 7 is another schematic diagram of a second re-distribution layer according to an example embodiment;

[0015] FIG. 8 is an enlarged view of a dashed-line box in FIG. 7 according to an example embodiment;

[0016] FIG. 9 is a schematic diagram of an extension portion and a vertical portion according to an example embodiment;

[0017] FIG. 10 is another schematic diagram of a second re-distribution layer according to an example embodiment;

[0018] FIG. 11 is another schematic diagram of a second re-distribution layer according to an example embodiment; and

[0019] FIG. 12 is a schematic diagram of a package component according to an example embodiment.

DESCRIPTION OF EMBODIMENTS

[0020] The technical solutions of the present disclosure are further described below in detail with reference to the accompanying drawings and the embodiments. Although example implementation methods of the present disclosure are shown in the accompanying drawings, it should be understood that the present disclosure may be implemented in various forms without being limited by the implementations described herein. Instead, these implementations are provided to develop a more thorough understanding of the present

disclosure and to fully convey the scope of the present disclosure to a person skilled in the art.

[0021] In the following paragraphs, the present disclosure is described more specifically by way of example with reference to the accompanying drawings. The advantages and features of the present disclosure will be clearer from the following description and claims. It should be noted that the accompanying drawings are presented in a highly simplified form and are not drawn to exact scale, and are merely intended to conveniently and clearly assist in describing the embodiments of the present disclosure.

[0022] It may be understood that meanings of "on", "over", and "above" in the present disclosure should be understood in the broadest sense, so that "on" means that it is "on" something with no intermediate feature or layer (that is, directly on something), and further includes the meaning that it is "on" something with an intermediate feature or layer.

[0023] In the embodiments of the present disclosure, the terms "first", "second", "third", and the like are intended to distinguish between similar objects but do not necessarily indicate a specific order or sequence.

[0024] In the embodiments of the present disclosure, the term "layer" refers to a material part including a region having a thickness. The layer may extend over the whole of a lower or upper structure, or may have a range smaller than the range of the lower or upper structure. In addition, the layer may be a region of a homogeneous or heterogeneous continuous structure whose thickness is less than the thickness of a continuous structure. For example, the layer may be located between the top surface and the bottom surface of the continuous structure, or the layer may be located between any horizontal surface pair at the top surface and the bottom surface of the continuous structure. The layer may extend horizontally, vertically, and/or along an inclined surface. The layer may include multiple sublayers.

[0025] It should be noted that the technical solutions described in the embodiments of the present disclosure may be randomly combined when there is no conflict.

[0026] With a trend of miniaturization of a package product, the thickness of a substrate greatly affects the size of a package structure. The substrate is usually formed by stacking multiple organic materials. To ensure the strength of the substrate, more organic material layers need to be stacked, which causes the substrate to become thicker, and further causes the thickness of the package structure become larger. This is inconducive to implementation

of a miniaturized product.

[0027] An embodiment of the present disclosure provides a package structure, and in the package structure, a re-distribution substrate serves as a support substrate. Because the re-distribution substrate is formed by deposition processes multiple times, the thickness of each film layer can be accurately controlled, and the thickness of a re-distribution layer can be further controlled, thereby reducing the thickness of the re-distribution substrate.

[0028] As shown in FIG. 1, an embodiment of the present disclosure provides a package structure 100. The package structure 100 may include dielectric layers 110, first re-distribution layers 120, second re-distribution layers 130, chips 140, wires 150, a molding layer 160, and an external terminal 170. The first re-distribution layers 120 are located in the dielectric layers 110. The second re-distribution layers 130 are located on the first re-distribution layers 120, and the tops of the second re-distribution layers 130 protrude from the dielectric layers 110. The dielectric layers 110, the first re-distribution layer 120, and the second re-distribution layer 130 may be re-distribution substrates. The chips 140 are located on the front surface of the dielectric layers 110, and are connected to the second re-distribution layers 130 through the wires 150. The molding layer 160 covers the chips 140 and the wires 150. The external terminal 170 is located on the back surface of the dielectric layers 110, and is connected to the first re-distribution layers 120, to implement external signal transmission. In this embodiment of the present disclosure, the wires 150 are directly welded to the second re-distribution layers 130, that is, the second re-distribution layers 130 serve as pads, so that no pad needs to be additionally disposed. In addition, because the thickness of the first re-distribution layers 120 and the thickness of the second re-distribution layers 130 are relatively small, the overall thickness of the dielectric layers 110 can be reduced, and the size of the package structure 100 is further reduced.

[0029] As shown in FIG. 2, the dielectric layers 110 may include a first dielectric layer 111, a second dielectric layer 112, a third dielectric layer 113, and a fourth dielectric layer 114 that are stacked in the vertical direction. The first dielectric layer 111 is located on the fourth dielectric layer 114, the second dielectric layer 112 is located on the first dielectric layer 111, and the third dielectric layer 113 is located on the second dielectric layer 112. When the dielectric layers 110 are formed, the first dielectric layer 111, the second dielectric layer 112,

and the third dielectric layer 113 may be first formed on a temporary substrate, and then the temporary substrate is removed, so that the fourth dielectric layer 114 is formed under the first dielectric layer 111. In this embodiment of the present disclosure, the materials from the first dielectric layer 111 to the fourth dielectric layer 114 may be the same. The material of the first dielectric layer 111 may be an insulating material, e.g., a thermosetting resin (such as epoxy resin), a thermoplastic resin (such as polyimide), or an insulating material in which these resins are impregnated in a core material (such as an inorganic filler and/or glass fiber (glass fiber, glass cloth, or glass fabric)) (e.g., prepreg, an Ajinomoto build-up film (ABF), FR-4, or bismaleimide triazine (BT)). The first dielectric layer 111 may further include a photosensitive resin such as photoimageable dielectric (PID) resin.

[0030] As shown in FIG. 2, the thickness of the first dielectric layer 111 is basically the same as the thickness of the second dielectric layer 112, the thickness of the second dielectric layer 112 is basically the same as the thickness of the third dielectric layer 113, and the thickness of the first dielectric layer 111 is greater than the thickness of the fourth dielectric layer 114. Because re-distribution layers need to be formed in the first dielectric layer 111, the second dielectric layer 112, and the third dielectric layer 113, and no re-distribution layer needs to be formed in the fourth dielectric layer 114, the thicknesses of the first dielectric layer 111 to the third dielectric layer 113 are relatively large. In addition, because the external terminal 170 is formed after the fourth dielectric layer 114, the thickness of the fourth dielectric layer 114 is relatively small, and etching time of the fourth dielectric layer 114 can be reduced. In this embodiment of the present disclosure, the thickness of the fourth dielectric layer 114 can be reduced, thereby reducing the overall thickness of the dielectric layers 110, reducing the size of the external terminal 170, and further reducing the thickness of the package structure 100. The thickness of the first dielectric layer 111 may be 9 μm–10 μm, the thickness of the fourth dielectric layer 114 may be 4 μm–5 μm, and the thickness of the fourth dielectric layer 114 may be equal to half of the thickness of the first dielectric layer 111. If the thickness of the fourth dielectric layer 114 is close to the thickness of the first dielectric layer 111, and the size of the external terminal 170 increases correspondingly, the overall thickness of the dielectric layer 110 increases. If the thickness of the fourth dielectric layer 114 is extremely small, e.g., 1 μm–2 μm, the fourth dielectric layer 114 cannot protect the first re-

distribution layers 120, which is inconducive to disposing the external terminal 170.

[0031] As shown in FIG. 2 to FIG. 3, there are the first re-distribution layers 120 in the dielectric layers 110. Each of the first re-distribution layers 120 may include a lower conductive pattern 121, an intermediate conductive pattern 122, and an upper conductive pattern 123. The lower conductive pattern 121 is located on the fourth dielectric layer 114. When the lower conductive pattern 121 is formed, the lower conductive pattern 121 is first formed on a temporary base, and then the first dielectric layer 111 is formed, so that the first dielectric layer 111 can cover the lower conductive pattern 121. The lower conductive pattern 121 may extend horizontally on the fourth dielectric layer 114. There is the intermediate conductive pattern 122 on the lower conductive pattern 121, and the intermediate conductive pattern 122 may include a vertical portion 1221 and a horizontal portion 1222. The vertical portion 1221 may be located in the first dielectric layer 111, to be electrically connected to the lower conductive pattern 121. The horizontal portion 1222 is located on the first dielectric layer 111, and extends horizontally on the first dielectric layer 111. In addition, in the vertical direction (the Y direction), the thickness of the vertical portion 1221 is greater than the thickness of the horizontal portion 1222. In this embodiment of the present disclosure, the intermediate conductive pattern 122 is formed after the first dielectric layer 111, so that the vertical portion 1221 can be formed in the first dielectric layer 111, and the horizontal portion 1222 is formed on the first dielectric layer 111. In this embodiment of the present disclosure, a sidewall of the vertical portion 1221 is inclined. By increasing the thickness of the vertical portion 1221, the upper width of the vertical portion 1221 may be increased, thereby being conducive to metal filling, further increasing a contact area with the horizontal portion 1222, and improving signal transmission performance. In some embodiments, each of the first re-distribution layers 120 may include a ground pattern, a power supply pattern, a signal pattern, and the like. The signal pattern may include various signals (such as data signals) other than those of the ground pattern and the power supply pattern associated with a power supply.

[0032] As shown in FIG. 2, after the intermediate conductive pattern 122 is formed, the second dielectric layer 112 is first formed on the first dielectric layer 111, the upper conductive pattern 123 is then formed on the second dielectric layer 112, and the upper conductive pattern 123 is electrically connected to the intermediate conductive pattern 122. The structure of the

upper conductive pattern 123 may be the same as the structure of the intermediate conductive pattern 122. A part of the upper conductive pattern 123 is located in the second dielectric layer 112, and a part of the upper conductive pattern 123 is located on the second dielectric layer 112. After the upper conductive pattern 123 is formed, the third dielectric layer 113 is formed on the second dielectric layer 122. The third dielectric layer 113 may cover a horizontal portion of the upper conductive pattern 123. It should be noted that a seed barrier layer is further formed between each of the dielectric layers 110 and each of the lower conductive pattern 121, the intermediate conductive pattern 122, and the upper conductive pattern 123, and the material of the seed barrier layer may be titanium or tantalum.

[0033] As shown in FIG. 2 and FIG. 4, after the third dielectric layer 113 is formed, the second re-distribution layers 130 may be further formed in the third dielectric layer 113. The tops of the second re-distribution layers 130 protrude from the top surface of the third dielectric layer 113, that is, in the vertical direction, the tops of the second re-distribution layers 130 are located outside the third dielectric layer 113. The tops of the second re-distribution layers 130 are located outside the third dielectric layer 113, that is, are located on the outside of the dielectric layers 110. Therefore, the second re-distribution layers 130 may serve as pads, and no pad needs to be additionally formed on the third dielectric layer 113.

[0034] As shown in FIG. 2 and FIG. 4, each of the second re-distribution layers 130 may include a body portion 131 and an extension portion 132. The body portion 131 may be located in the third dielectric layer 113. The extension portion 132 may be located on the body portion 131, and extends to the third dielectric layer 113, that is, the extension portion 132 is located on the third dielectric layer 113. The extension portion 132 may be the top of each of the second re-distribution layers 130. In the vertical direction, the thickness of the extension portion 132 is less than the thickness of the body portion 131. Because wire bonding is further required on the second re-distribution layers 130, the tops of the second re-distribution layers 130 need to be lower than the chips 140. In this case, the extension portion 132 with a relatively small thickness is formed. Certainly, each of the second re-distribution layers 130 may further include a metal layer 133, the metal layer 133 is located on the extension portion 132, and the metal layer 133 is conformally located on the extension portion 132. "Conformally" may be understood as that the metal layer 133 may continue to grow on the

top surface of the extension portion 132. For example, the top surface of the extension portion 132 is horizontal, and in this case, the top surface of the metal layer 133 is also horizontal. For another example, the top surface of the extension portion 132 is inclined, and in this case, the top surface of the metal layer 133 is also inclined. Each of the wires 150 may be connected to the metal layer 133. It should be noted that there is a seed barrier layer between the body portion 131 and each of the dielectric layers 110, and there is also a seed barrier layer between the extension portion 132 and each of the dielectric layers 110.

[0035] As shown in FIG. 2 and FIG. 4, the metal layer 133 is located on the top surface of the extension portion 132, that is, the metal layer 133 is not located on a sidewall of the extension portion 132. There are a large quantity of second re-distribution layers 130 on the dielectric layers 110, and these second re-distribution layers 130 are regularly arranged. The metal layer 133 is located on the top surface of the extension portion 132. In this case, a spacing between adjacent ones of the second re-distribution layers 130 can be appropriately reduced, so that a quantity of the second re-distribution layers 130 can be increased, thereby providing better signal transmission for the chips.

[0036] As shown in FIG. 2 and FIG. 4, the material of the body portion 131 and the material of the extension portion 132 are the same, and the material of the extension portion 132 and the material of the metal layer 133 are different. Because each of the wires 150 is connected to the metal layer 133, the material of the metal layer 133 and the material of the wires 150 are the same. In addition, the body portion 131 is electrically connected to the upper conductive pattern 123. However, the material of the body portion 131 is different from the material of the upper conductive pattern 123, and the hardness of either of the body portion 131 and the extension portion 132 may be greater than the hardness of the upper conductive pattern 123. After each of the wires 150 is connected to the metal layer 133, the endpoint of each of the wires 150 needs to be cut off by utilizing a dicing blade, and the dicing blade exerts an acting force on the body portion 131. Therefore, the body portion 131 and the extension portion 132 need to have a higher hardness, to prevent the body portion 131 from being deformed. In this embodiment of the present disclosure, the material of the body portion 131 may be nickel or titanium, the material of the upper conductive pattern 123 may be copper or aluminum, and the material of the metal layer 133 may be gold.

[0037] As shown in FIG. 1 and FIG. 5, the chips 140 are disposed on the front surface of the dielectric layers 110, and the chips 140 are connected to the second re-distribution layers 130 through the wires 150. The quantity of the chips 140 may be multiple, e.g., two, four, eight, or more. Each of the chips 140 may be a logic chip or a memory chip. The logic chip may include, e.g., a central processing unit (CPU), an image processing unit (GPU), a field programmable gate array (FPGA), a digital signal processor (DSP), an encryption processor, a microprocessor, a microcontroller, an analog-to-digital converter, and an application-specific integrated circuit (ASIC). The memory chip may include, e.g., a volatile memory apparatus (such as a dynamic random access memory (DRAM), a static RAM (SRAM)), or a non-volatile memory apparatus (such as a phase change RAM (PCRAM), a magnetic RAM (MRAM), a resistive RAM (RRAM), or a flash memory). In this embodiment, four chips 140 are disposed, which are respectively a first chip 141 to a fourth chip 144. The first chip 141 to the fourth chip 144 are stacked in sequence. The first chip 141 is located on the third dielectric layer 113, the second chip 142 is offset on the first chip 142, the third chip 143 is offset on the second chip 142, and the fourth chip 144 is offset on the third chip 143. An offset direction of the second chip 142 and an offset direction of the third chip 143 are the same, for example, offset to the right in FIG. 5, and an offset direction of the fourth chip 144 is opposite to the offset direction of the third chip 143, for example, offset to the left in FIG. 5. The first chip 141 is connected to the second chip 142 through one of the wires 150, and the first chip 141 is connected to the second re-distribution layers 130 through one of the wires 150. The fourth chip 144 is connected to the third chip 143 through one of the wires 150, and the third chip 143 is connected to the second re-distribution layers 130 through one of the wires 150. Because the first chip 141 to the fourth chip 144 are chips of the same specification, e.g., DRAM chips of the same model, the length of the lead 150 from the second chip 142 to the first chip 141 is the same as the length of the lead 150 from the fourth chip 144 to the third chip 143. The distance between the first chip 141 and the third dielectric layer 113 may be the thickness of the first chip 141, and the distance between the third chip 143 and the third dielectric layer 113 may be the sum of the thicknesses of the first chip 141 to the third chip 143. The first chip 141 is lower than the third chip 143. In this case, the length of the lead 150 between the first chip 141 and the second re-distribution layers 130 is less than the length of

the lead 150 between the third chip 143 and the second re-distribution layers 130. Consequently, there is a time difference in signal transmission on the first chip 141 and the third chip 143, causing inconsistent signal transmission. In this embodiment of the present disclosure, a first distance d1 between the second re-distribution layers 130 on the left side and the first chip 141 is greater than a second distance d2 between the second re-distribution layers 130 on the right side and the third chip 143, to reduce the length difference between wires 150 on the left side and the right side, and further reduce the time difference of the signal transmission. In this embodiment of the present disclosure, the second distance d2 between the second re-distribution layers 130 on the right side and the third chip 143 may be 240 um–250 um, and the first distance d1 between the second re-distribution layers 130 on the left side and the first chip 141 may be 300 um–350 um. In other words, the difference between the first distance d1 and the second distance d2 is basically equal to the sum of thicknesses of the second chip 142 and the third chip 143.

[0038] As shown in FIG. 5, after the wires 150 are formed, the molding layer 160 may be further formed on the third dielectric layer 113, and the molding layer 160 covers the first chip 141 to the fourth chip 144, and further covers the wires 150. The molding layer 160 may protect the chips 140. The molding layer 160 may include an insulating material. Examples of the insulating material may include a thermosetting resin (such as epoxy resin), a thermoplastic resin (such as polyimide), a prepreg including an inorganic filler and/or a glass fiber, an Ajinomoto build-up film (ABF), FR-4, bismaleimide triazine (BT), an epoxy molded compound (EMC), or the like.

[0039] As shown in FIG. 2 and FIG. 5, after the molding layer 160 is formed, a temporary substrate is disposed on the surface of the molding layer 160, and the temporary substrate is flipped. In this case, the fourth dielectric layer 114 may be formed on the first dielectric layer 111, and then a part of the fourth dielectric layer 114 is etched, to form the external terminal 170 in the fourth dielectric layer 114. The external terminal 170 may be electrically connected to the lower conductive pattern 121, to implement signal transmission. The external terminal 170 may be a solder ball or a bump.

[0040] As shown in FIG. 1, in this embodiment of the present disclosure, when the second re-distribution layers 130 are formed, the chips 140 are connected to the second re-distribution

layers 130 through the wires 150, instead of fastening the chips 140 to the second re-distribution layers 130 through solder balls. When the solder balls are utilized to fasten the chips 140, the molding material needs to enter among the chips 140 and the dielectric layers 110 during molding. In a case in which the density of each of the solder balls is increasingly larger and the size of each of the solder ball is increasingly smaller, it is difficult for the molding material to enter among the chips 140 and the dielectric layers 110, and it is easy to form a gap in the molding layer 160, consequently degrading the performance of the molding layer 160. In addition, each of the solder balls has a specific height. If the solder balls are utilized to fasten the chips 140, the overall height of the package structure 100 increases. In this embodiment, the chips 140 are bonded to the dielectric layers 110, and then the chips are connected to the second re-distribution layers 130 through the wires 150, so that the molding layer 160 can completely cover the chips 140. In addition, the overall height of the package structure 100 can be reduced. In addition, the overall thickness of the dielectric layer 110 decreases, so that the overall thickness of the package structure can be reduced.

[0041] As shown in FIG. 1, in this embodiment of the present disclosure, the tops of the second re-distribution layers 130 are outside the dielectric layers 110, and the wires 150 may be directly connected to the second re-distribution layers 130. If the tops of the second re-distribution layers 130 are inside the dielectric layers 110, that is, the second re-distribution layers 130 are lower than the dielectric layers 110, parts of the dielectric layers 110 protruding from the second re-distribution layers 130 may affect a press-fit procedure of the wires 150. In addition, when the wires 150 are laid on the second re-distribution layers 130, the lengths of the wires 150 are also lengthened. In a subsequent molding procedure, a molding material needs to be filled in the dielectric layers 110, consequently causing swinging of the wires 150 and degrading the stability of the wires 150. In this embodiment of the present disclosure, the tops of the second re-distribution layers 130 are outside the dielectric layers 110, and the second re-distribution layers 130 do not block a wire bonding procedure. In this embodiment of the present disclosure, the lengths of the wires 150 can be further reduced. In addition, the second re-distribution layers 130 slow down the flow speed of the molding material, reducing the impact on the wires 150, and improving the stability of the wires 150.

[0042] As shown in FIG. 2, in this embodiment of the present disclosure, the first

dielectric layer 111, the second dielectric layer 112, and the third dielectric layer 113 are respectively formed by deposition processes multiple times. The deposition processes can improve the precision of the first dielectric layer 111 to the third dielectric layer 113, reduce the thicknesses of the first dielectric layer 111 to the third dielectric layer 113, further reduce the thicknesses of the dielectric layers 110, and then reduce the thickness of the package structure 100. In this embodiment of the present disclosure, an organic substrate is not utilized. The organic substrate needs to be formed by stacking multiple organic sub-substrates, and then a conductive line is formed through drilling. In this case, the thickness of the organic substrate is relatively large, which is inconducive to reducing the thickness of the package structure 100.

[0043] As shown in FIG. 6, an embodiment of the present disclosure provides another package structure 100. A difference between the package structure 100 and that in FIG. 1 lies in that the structure of each of the second re-distribution layers 130 in FIG. 6 is different from the structure of each of the second re-distribution layers 130 in FIG. 1. For the structure of each of dielectric layers 110, first re-distribution layers 120, chips 140, wires 150, a molding layer 160, and an external terminal 170 in FIG. 6, refer to the foregoing descriptions. The structure of each of the second re-distribution layers 130 is mainly described herein.

[0044] As shown in FIG. 7 and FIG. 8, each of the second re-distribution layers 130 includes a body portion 131, an extension portion 132, and a metal layer 133. The body portion 131 is located in a third dielectric layer 113, and the extension portion 132 is located on the body portion 131, and extends to the third dielectric layer 113. The top surface of the extension portion 132 is inclined, and the metal layer 133 is conformally formed on the extension portion 132. In this case, the top surface of the metal layer 133 is also inclined. It may be learned from FIG. 8 that in the vertical direction, an end portion of the extension portion 132 close to one of the chips 140 has a relatively large thickness, and an end portion of the extension portion 132 away from the chip 140 has a relatively small thickness. The maximum thickness of the extension portion 132 is less than the thickness of the body portion 131. The maximum thickness of the extension portion 132 is far less than the thicknesses of the chips 140. In this embodiment of the present disclosure, the maximum thickness of the extension portion 132 is approximately equal to 1/10 of the thicknesses of the chips 140. If

the maximum thickness of the extension portion 132 is excessively large, it is inconducive to a wire bonding procedure of the wires 150. It may be learned from FIG. 8 that the top surface 1331 of the metal layer 133 is inclined, that is, the top surface 1331 is inclined relative to the surface of the third dielectric layer 113. In this case, an included angle between the top surface 1331 and the third dielectric layer 113 may be an angle b. An end portion of one of the wires 150 is on the top surface 1331, and in this case, there is an included angle between the lead 150 and the top surface 1331, namely, an angle a. The included angle between the lead 150 and the top surface 1331 may be understood as an included angle between the tangent of the lead 150 and the top surface 1331. In this embodiment of the present disclosure, the angle a may be greater than the angle b, that is, the top surface 1331 is relatively flat, that is, the top surface of the extension portion 132 is relatively flat. In this case, the thickness of the end portion of the extension portion 132 close to one of the chips 140 is relatively small, which is conducive to wire bonding. During wire bonding, to ensure that the wires 150 have good radians and ensure that the wires 150 have good stability, the range of the angle a should be relatively large, and the angle a may be greater than the angle b. In addition, when the end portion of the lead 150 is led onto the metal layer 133, a dicing blade needs to be utilized to press-fit the lead 150. Because the bottom of the dicing blade is arc-shaped, the flat top surface 1331 is disposed, so that the cut surface of the bottom of the dicing blade is basically parallel to the top surface 1331. When press-fitting and cutting are performed by the dicing blade, the lead 150 can be pressed as a whole, thereby improving the uniformity and the stability of press-fitting and shaping the lead, and further improving the stability of the lead 150. In this embodiment of the present disclosure, the angle b may range from 8° to 10°, for example, be 9°, and the angle a may range from 15° to 20°, for example, be 16° or 17°.

[0045] As shown in FIG. 7 and FIG. 8, in this embodiment of the present disclosure, the thickness of the end portion of the extension portion 132 close to one of the chips 140 is greater than the thickness of the end portion of the extension portion 132 away from the chip 140, thereby being conducive to a press-fit procedure of the wires 150. If the thickness of the end portion of the extension portion 132 close to one of the chips 140 is less than the thickness of the end portion of the extension portion 132 away from the chip 140, the angle a between the lead 150 and the top surface 1331 becomes larger, and the bottom surface of a dicing blade

cannot be well matched to the lead 150. In this case, it is inconducive to a press-fit procedure of the wires 150, and inconducive to forming stable wires 150.

[0046] As shown in FIG. 7 and FIG. 8, in this embodiment of the present disclosure, the inclined extension portion 132 is formed, to further form the inclined metal layer 133, so that the stability of the wires 150 can be improved in the press-fit procedure of the wires 150.

[0047] As shown in FIG. 9, figure (a) is a simplified schematic diagram of an extension portion 132, and figure (b) is a simplified schematic diagram of a vertical portion 221. The top surface 1321 of the extension portion 132 is inclined, and a sidewall 1221a of the vertical portion 1221 is inclined. The top surface 1321 of the extension portion 132 can be conducive to the stability of the wires 150, and the sidewall 1221a of the vertical portion 1221 can be conducive to metal filling. In addition, the sidewall 1221a of the extension portion 1221 has a first slope, the top surface 1321 of the extension portion 132 has a second slope, and the absolute value of the first slope is greater than the absolute value of the second slope. The angle of the first slope is less than 90°. If the absolute value of the first slope is less than the absolute value of the second slope, that is, the angle of the second slope is greater, the top surface 1321 becomes steep, which is inconducive to a formation procedure of the wires 150.

[0048] As shown in FIG. 10, an embodiment of the present disclosure further provides another second re-distribution layer 130, and no metal layer is displayed in the second re-distribution layer 130. The second re-distribution layer 130 includes a body portion 131 and an extension portion 132. The extension portion 132 is located on the body portion 131. The extension portion 132 has an inclined surface. In the vertical direction, an end portion of the extension portion 132 close to one of the chips 140 has a relatively large thickness, and an end portion of the extension portion 132 away from the chip 140 has a relatively small thickness. A center line S2 of the extension portion 132 is offset from a center line S1 of the body portion 131. In addition, the center line S2 of the extension portion 132 is closer to the chips 140, that is, the center line S2 of the extension portion 132 is offset to the chips 140. In other words, it may be learned from FIG. 10 that the distance from an end portion of the extension portion 132 at the right side to the body portion 131 is greater than the distance from an end portion of the extension portion 132 at the left side to the body portion 131. The distance from an end portion of the extension portion 132 with a larger thickness to the chips

140 is closer. Therefore, it is conducive to a press-fit procedure of the wires of the chips 140, improving the stability and the uniformity of the wires.

[0049] As shown in FIG. 11, an embodiment of the present disclosure further provides another second re-distribution layer 130. The second re-distribution layer 130 may include a body portion 131, an extension portion 132, and a recessed portion 134. An opening may be formed in the third dielectric layer 113. In an electroplating procedure, an inner wall of the opening and the top surface of the third dielectric layer 113 simultaneously grow metal materials, and the opening has a specific depth. In the electroplating procedure, an electroplating solution inside the opening is not updated in a timely manner, and metal ions cannot be deposited in the opening in a timely manner. In this case, a metal layer inside the opening slowly grows. In this case, the recessed portion 134 is formed in the extension portion 132 and the body portion 131, that is, the recessed portion 134 is located in the extension portion 132 and the body portion 131, and extends from the extension portion 132 to the body portion 131. The body portion 131 is still located in the third dielectric layer 113, and the extension portion 132 is located on the top surface of the third dielectric layer 113, that is, the extension portion 132 protrudes from the third dielectric layer 113. The existence of the recessed portion 134 is inconducive to an operation procedure of the wires. Therefore, in this embodiment, a gold ball 135 is formed in the recessed portion 134. In this case, the gold ball 135 may serve as a part of the second re-distribution layer 130, that is, the second re-distribution layer 130 includes the gold ball 135. The gold ball 135 may be in contact with a sidewall of the recessed portion 134, and may be further in contact with the bottom surface of the recessed portion 134. The gold ball 135 is located in the recessed portion 134, and there is still a gap between the gold ball 135 and the sidewall of the recessed portion 134. Certainly, in some embodiments, the bottom of the gold ball 135 may be further deformed, so that no gap exists between the gold ball 135 and the sidewall of the recessed portion 134, that is, a contact area between the gold ball 135 and the recessed portion 134 can be increased. In addition, the top surface of the gold ball 135 is higher than the top surface of the extension portion 132, that is, the height of the gold ball 135 is greater than the depth of the recessed portion 134. Because the gold ball 135 is higher, the wires 150 can be directly press-fit on the gold ball 135. Because the materials of the gold ball 135 and the wires 150 are the same, a

binding force is relatively high, which is conducive to a wire bonding procedure. In addition, when the wires 150 are press-fit on the gold ball 135, a binding force between the gold ball 135 and the recessed portion 134 may be further increased. In some embodiments, the height of the gold ball 135 may be 2 μm greater than the depth of the recessed portion 134. The height of the gold ball 135 is, e.g., 8 μm–10 μm, and the depth of the recessed portion 134 is, e.g., 6 μm–8 μm.

[0050] As shown in FIG. 1, an embodiment of the present disclosure further provides a package structure 100. The package structure 100 may include dielectric layers 110, first re-distribution layers 120, second re-distribution layers 130, chips 140, and wires 150. The first re-distribution layers 120 are located in the dielectric layers 110, the second re-distribution layers 130 are located on the first re-distribution layers 130, the first re-distribution layers 120 are electrically connected to the second re-distribution layers 130, and the tops of the second re-distribution layers 130 protrude from the dielectric layers 110. The chips 140 are located on the dielectric layers 110, and the wires 150 connect the chips 140 to the second re-distribution layers 130. The dielectric layers 110 may include a first dielectric layer 111 to a fourth dielectric layer 114. The first dielectric layer 111 is located on the fourth dielectric layer 114, the second dielectric layer 112 is located on the first dielectric layer 111, and the third dielectric layer 113 is located on the second dielectric layer 112. The thicknesses of the first dielectric layer 111 to the third dielectric layer 113 are the same, and the thickness of the fourth dielectric layer 114 is less than the thickness of the first dielectric layer 111. The dielectric layers 110 in the package structure 100 may have a smaller thickness, so that the package structure 100 can have a smaller package volume.

[0051] As shown in FIG. 12, an embodiment of the present disclosure provides a package component 10. The package component 10 may include a substrate 200 and a package structure 100. The substrate 200 is, e.g., a PCB, a flexible substrate, or a strip substrate. For the package structure 100, refer to the foregoing structure. The package structure 10 may be applied to an electronic device. The electronic device may include one or more of the following: e.g., a smart phone, a tablet personal computer (PC), a mobile phone, a video phone, an e-book (e-book) reader, a desktop PC, a laptop PC, a netbook computer, a workstation, a server, a personal digital assistant (PDA), a portable multimedia player (PMP), an MPEG-1

audio layer 3 (MP3) player, a mobile medical device, a camera, a home appliance, a medical device, an Internet of Things (IoT) device, and a wearable device. The wearable device may be of an accessory type, a fabric or clothing type, a body attachment type, or an implantable circuit type. An accessory-type wearable device may be, e.g., a watch, a ring, a bracelet, an anklet, a necklace, glasses, contact lenses, or a head-mounted device (HMD).

[0052] In conclusion, the embodiments of the present disclosure provide the package structure and the package component. A relatively small re-distribution substrate is utilized to support the chips, so that the thickness of the package structure can be reduced. In addition, because the tops of the second re-distribution layers protrude from the dielectric layers, it is conducive to directly connecting the wires to the second re-distribution layers, and conducive to the formation procedure of the wires.

[0053] The foregoing descriptions are merely specific implementations of the present disclosure, but are not intended to limit the protection scope of the present disclosure. Any variation or replacement readily figured out by a person skilled in the art within the technical scope disclosed in the present disclosure shall fall within the protection scope of the present disclosure. Therefore, the protection scope of the present disclosure shall be subject to the protection scope of the claims.

CLAIMS

What is claimed is:

1. A package structure, comprising:

dielectric layers;

first re-distribution layers, located in the dielectric layers;

second re-distribution layers, located on the first re-distribution layers, the first re-distribution layers being electrically connected to the second re-distribution layers, and tops of the second re-distribution layers protruding from the dielectric layers;

chips, located on the dielectric layers; and

wires, connecting the chips to the second re-distribution layers.

2. The package structure according to claim 1, wherein each of the second re-distribution layers comprises:

a body portion, located in one of the dielectric layers; and

an extension portion, located on the body portion and extending to a top surface of one of the dielectric layers.

3. The package structure according to claim 2, wherein in a vertical direction, a thickness of the body portion is greater than a thickness of the extension portion.

4. The package structure according to claim 2 or 3, wherein in a horizontal direction, there is an included angle between a top surface of the extension portion and the top surface of one of the dielectric layers.

5. The package structure according to claim 4, wherein a thickness of an end portion of the extension portion close to one of the chips is greater than a thickness of an end portion of the extension portion away from the chip.

6. The package structure according to claim 4, wherein a center line of the extension portion is offset from a center line of the body portion, and the center line of the extension portion is offset toward the chips.

7. The package structure according to any one of claims 2 to 6, wherein each of the second re-distribution layers further comprises:

a metal layer, conformally disposed on the extension portion, wherein

a thickness of the metal layer is less than the thickness of the extension portion.

8. The package structure according to claim 7, wherein one of the wires is connected to the metal layer, and an angle between the metal layer and the lead is greater than an included angle between a top surface of the metal layer and the top surface of one of the dielectric layers.

9. The package structure according to any one of claims 1 to 3, wherein the first re-distribution layer comprises:

a lower conductive pattern, located at a bottom of one of the dielectric layers, wherein the lower conductive pattern extends horizontally in the dielectric layer;

an intermediate conductive pattern, located in a middle part of one of the dielectric layers, and connected to the lower conductive pattern; and

an upper conductive pattern, located on an upper part of one of the dielectric layers, and connected to the intermediate conductive pattern.

10. The package structure according to claim 9, wherein a material of the body portion is different from a material of the upper conductive pattern, and a hardness of the body portion is greater than a hardness of the upper conductive pattern.

11. The package structure according to claim 9, wherein the intermediate conductive pattern comprises:

a vertical portion, connected to the lower conductive pattern; and

a horizontal portion, connected to the vertical portion, and extending horizontally in one of the dielectric layers, wherein

in the vertical direction, a thickness of the vertical portion is greater than a thickness of the horizontal portion; and

in the horizontal direction, a width of the vertical portion is less than a width of the body portion.

12. The package structure according to claim 11, wherein a sidewall of the vertical portion has a first slope, a top surface of the extension portion has a second slope, and an absolute value of the first slope is greater than an absolute value of the second slope.

13. The package structure according to claim 11, wherein the body portion is connected to the upper conductive pattern, and the thickness of the body portion is greater than the thickness of the horizontal portion.

14. The package structure according to any one of claims 1 to 3, wherein the second re-distribution layers are located on two sides of the chips, and spacings from the second re-distribution layers on the two sides to the chips are different.

15. The package structure according to claim 2, wherein each of the second re-distribution layers further comprises:

a recessed portion, extending from the extension portion to the body portion; and

a gold ball, located in the recessed portion, wherein one of the wires is connected to the gold ball, wherein

a height of the gold ball is greater than a depth of the recessed portion.

16. The package structure according to any one of claims 1 to 3, wherein the chips comprise:

a first chip, located on one of the dielectric layers;

a second chip, offset on the first chip;

a third chip, offset on the second chip; and

a fourth chip, offset on the third chip, wherein

an offset direction of the second chip and an offset direction of the third chip are the same, and an offset direction of the fourth chip is opposite to the offset direction of the third chip.

17. The package structure according to claim 16, wherein the first chip is connected to the second chip through one of the wires, the first chip is connected to one of the second re-distribution layers through one of the wires, the fourth chip is connected to the third chip through one of the wires, and the third chip is connected to one of the second re-distribution layers through one of the wires.

18. The package structure according to claim 17, wherein a length of the lead from the second chip to the first chip is equal to a length of the lead from the fourth chip to the third chip.

19. The package structure according to claim 17, wherein a first distance from one of the second re-distribution layers to the first chip is greater than a second distance from one of the second re-distribution layers to the third chip.

20. A package structure, comprising:

dielectric layers;

first re-distribution layers, located in the dielectric layers;

second re-distribution layers, located on the first re-distribution layers, the first re-distribution layers being electrically connected to the second re-distribution layers, and tops of the second re-distribution layers protruding from the dielectric layers;

chips, located on the dielectric layers; and

wires, connecting the chips to the second re-distribution layers;

wherein the dielectric layers comprising:

a first dielectric layer, located on a fourth dielectric layer;

a second dielectric layer, located on the first dielectric layer; and

a third dielectric layer, located on the second dielectric layer, a thickness of the third dielectric layer being equal to a thickness of the first dielectric layer, a thickness of the fourth dielectric layer being less than the thickness of the first dielectric layer, and the thickness of the first dielectric layer being equal to a thickness of the second dielectric layer.