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PATENT SPECIFICATION

DRAWINGS ATTACHED

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COMPLETE SPECIFICATION

Semiconductor Device

We, RADIO CORPORATION OF AMERICA, a corporation organised under the laws of the State of Delaware, United States of America, of 30 Rockefeller Plaza, City and State of New York, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates generally to semiconductive devices, and more particularly to an improved transistor having improved reverse-bias second breakdown and voltage ratings. The improved transistor of the present invention is particularly useful as a high frequency, power transistor of the type used in regulated power supplies, converters, inverters, amplifiers, and the like.

When current in a circuit employing a transistor and an inductive load is suddenly interrupted, a resulting induced voltage may cause the collector space charge layer in the transistor to spread through the active collector region of the transistor, the active collector region being that portion of the collector material beneath the base region and above the highly doped substrate of the transistor. If this occurs, base widening results and the possibility of a second voltage breakdown, depending on the impurity level of the substrate, is presented. This condition, if allowed to persist, would greatly reduce the transistor output impedance, and large currents would flow. Such action would produce an excessive heating of the transistor, resulting in its eventual destruction. The resulting induced voltage of an inductive load may also cause a very high current to flow through the collector region of the transistor under breakdown voltage conditions. Thus, a high current density and a high electric field may exist at the collector junction simultaneously. In some transistors, these conditions may precipitate a localized thermal runaway. This is especially true when crystallographic defects and/or non-uniform impurity regions exist in the base of the active collector regions of the transistor. Under these conditions, second breakdown is said to occur in the transistor. If the transistor's emitter-base junction is not forward biased, as in the case where an inductive circuit is suddenly interrupted, the second breakdown is referred to as a reverse-bias second breakdown.

In general, second breakdown in a junction transistor is a condition in which the output impedance changes instantaneously from a very large positive value to a negative value, then to a final small positive value. In some respects, the second breakdown appears similar to a normal avalanche breakdown, either collector-to-base or collector-to-emitter.

Physically, second breakdown is a local thermal runaway effect induced by severe current concentrations in the transistor. These concentrations of current can result from improper biasing conditions, excessive transverse base fields, or defects in the base region and/or junctions.

Second breakdown can occur to some degree in all junction transistors. In many low frequency and low-power transistors, for example, the maximum steady state dissipation rating limits the voltage-current product to something less than the critical value necessary to produce second breakdown. In relatively high-frequency, high-power transistors, however, the increased criticalness of their structural tolerances and the increased severity of their operating conditions cause them to have relatively lower second breakdown power ratings.

According to the present invention there is provided a semiconductor device having an emitter region of one conductivity type, a base region of an opposite conductivity type, and a collector region of said one conductivity type disposed adjacent said base region, said collector region comprising at least three layers

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having resistivities that decrease stepwise respectively in the direction away from said base region, the layer next to said base region having a thickness equal or substantially equal to that of the adjacent layer.

The novel features of the invention, as well as the invention itself, both as to its organization and method of operation, will be understood more fully when considered in connection with the accompanying drawing, the single figure of which is a fragmentary, cross-sectional view of the improved transistor.

Referwring now to the drawing, there is shown a fragment of an improved NPN transistor 10 of semi-conductive material, such as silicon or germanium, for example, comprising a combined collector region 14, a base region 16, and an emitter region 18.

While the transistor 10 is of the NPN type, it is merely illustrative of one embodiment of the invention, and it is also within contemplation of the present invention to provide improved PNP transistors with improved second breakdown characteristics.

The combined collector region 14 comprises a substrate collector layer 20 of degenerate semiconductive material, such as a wafer of highly doped, N type, monocrystalline silicon, indicated in the drawing by the symbol N+. The dimensions and resistivities given for the illustrated embodiment herein are for improved transistors of the 2N3265 type (medium voltage, high power, mesa NPN silicon transistors). The thickness of the substrate collector layer 20 is between 6.5 and 7.0 mils and its resistivity is less than 0.01 ohm-cm. These specifications are not critical and transistors of other types employing the improved structure may have different dimensions and resistivities.

The combined collector region 14 comprises, in addition to the substrate collector layer 20, at least two superimposed collector layers 22 and 24, of different resistivities, respectively, preferably formed by successive epitaxial depositions, on the substrate collector layer 20. For example, the collector layer 22 may have a thickness of 0.7 mil and a resistivity between 1.5 and 3 ohm-cm., and the collector layer 24 may have a thickness of about 0.7 mil and a resistivity between 9 and 15 ohm-cm. While only the three layers 20, 22, and 24 are shown herein as comprising the collector region 14, it is within the contemplation of the invention to provide more than three collector layers for the combined collector region 14, wherein the further each collector layer is from the base region 16, the lower is its respective resistivity. The resistivity of each collector layer may also vary slightly within each layer.

The layer 24 next to the base region, however, should have the same or substantially the same thickness as that of the next adjacent layer, that is, layer 22. Also, the resistivity of the layer 20 as noted in the aforementioned examples is less than 1/100 of that of the layer 24, and the resistivity of the layer 24 is at least three times greater than that of layer 22.

While the collector layers 22 and 24 have been described herein as being separately formed, epitaxial layers, such a method of manufacture being a preferred one, it is within the contemplation of the invention to substitute a single, epitaxially deposited layer, having a thickness and stepwise resistivity similar to that of the combined layers 22 and 24, for the layers 22 and 24. Such a stepwise resistivity in a single collector layer can be obtained by controlling the concentration of the dopant, such as phosphorus pentoxide, during the epitaxial deposition of the layer on the substrate collector layer 20.

The base region 16 may be easily formed in the collector layer 24 by diffusing a P type dopant into the layer 24 to a depth of about 0.2 mil, by any means well known in the transistor art. The junction of the base region 16 and the collector layer 24 form a PN rectifying junction 26.

An N type dopant is diffused into a portion of the base region 16 to a depth of about .1 mil, by any means known in the art, to provide the emitter region 18. The emitter region 18 is heavily doped by an N type dopant and is designated by the symbol N+ in the drawing. The emitter region 18 may also be formed by an alloying process well known in the art.

The resistivity of the collector layer 24 controls the avalanche breakdown voltage of the collector-base junction 26 of the transistor and, hence, determines the transistor's breakdown voltage characteristics. The thickness of the collector layer 24 determines the allowable space-charge widening, which, if impeded, would lower the voltage breakdown. The thickness of the collector layer 24 also determines the largest part of the transistor's collector series resistance, a function of the current-carrying capacity of the transistor 10. For any particular application of the transistor 10, the resistivity and thickness of the collector layer 24 should provide the highest voltage breakdown rating commensurate with a minimum of collector series resistance.

The resistivity of the collector layer 22 is a function of the maximum current density before reverse-bias second breakdown of the transistor occurs. The thickness of the collector layer 22 is a function of the permissible widening of the collector space charge layer. Hence, the resistivity and thickness of the collector layer 22 determine the magnitude of reverse-bias second breakdown protection of which the transistor 10 is capable. The resistivity-thickness product should be kept small so as to keep the saturation resistance low and thereby enhance the current-carrying capacity of the transistor 10. The resistivity of the collector layer 22, however, should be high enough to

prevent it from limiting the transistor's voltage ratings.

In operation, the collector layer 22 of the collector region 14 retards the spreading of the collector space charge layer to prevent it from contacting the heavily doped substrate layer 20 in the area where currents of high density are flowing. The collector layer 24 of the collector region 14 provides a thickness necessary to support at least one-half of a space charge layer at a theoretical breakdown voltage for a given resistivity. By employing three collector layers 20, 22 and 24 whose resistivities increase stepwise, respectively, towards the base region 16, the collector layer 22 functions as a distinct buffer in a zone where high current densities occur and thereby reduces the possibility of second breakdown.

From the foregoing description, it is apparent that there has been provided an improved transistor employing a collector region whose resistivity decreases stepwise, in the direction away from its base region. The improved transistor provides a relatively low saturation resistance and relatively high reverse-bias second breakdown energy capability. While only one one example of the improved transistor has been described in detail, variations in its structure, as well as in the methods of making it, all coming within the scope of this invention, will, no doubt, readily suggest themselves to those skilled in the art. Hence, it is desired that the foregoing description shall be considered as illustrative and not in a limiting sense.

WHAT WE CLAIM IS:—

1. A semiconductor device having an emitter region of one conductivity type, a base region of an opposite conductivity type, and a collector region of said one conductivity type disposed adjacent said base region, said collector region comprising at least three layers having resistivities that decrease stepwise respectively in the direction away from said base region, the layer next to said base region having a thickness equal or substantially equal to that of the adjacent layer.

2. A device as claimed in claim 1, wherein said adjacent layer is next to a substrate layer of degenerate semiconductor material of said collector region.

3. A device as claimed in claim 2, wherein said adjacent layer is an epitaxial layer formed on said substrate layer.

4. A device as claimed in claim 2 or 3, wherein said base region is diffused in said layer next to the base region and said emitter region is diffused in said base region.

5. A device as claimed in claim 2, 3 or 4 wherein said substrate layer has a resistivity that is less than one-hundredth of that of the layer next to the base region.

6. A semiconductor transistor substantially as hereinbefore described with reference to the accompanying drawing.

For the Applicants,
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4. A device as claimed in claim 2 or 3, wherein said base region is diffused in said layer next to the base region and said emitter region is diffused in said base region.

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