

STORAGE DEVICE AND ACCESS METHOD

ABSTRACT OF THE DISCLOSURE

A storage device and access method for performing hierarchical coding without the need for employing a circuit for a line delay, in addition to a memory for storing an image. An address providing circuit provides a 9-bit horizontal address and a 9-bit vertical address, as an address, to a first layer memory while providing, to a second layer memory, higher order eight bits of the horizontal address and the vertical address without respective least significant bits. As a result, at the timing each of the pixels in the first layer is written on each of addresses $(2s, 2t)$, $(2s+1, 2t)$, $(2s, 2t+1)$ and $(2s+1, 2t+1)$ in the first layer memory, the same address (s, t) in the second layer memory is accessed. Taking advantage of this, a read-modify-write circuit determines the sum of storage values at addresses $(2s, 2t)$, $(2s+1, 2t)$, $(2s, 2t+1)$, and $(2s+1, 2t+1)$ in the first layer memory and writes the sum onto the address (s, t) in the second layer memory.

Figure 1