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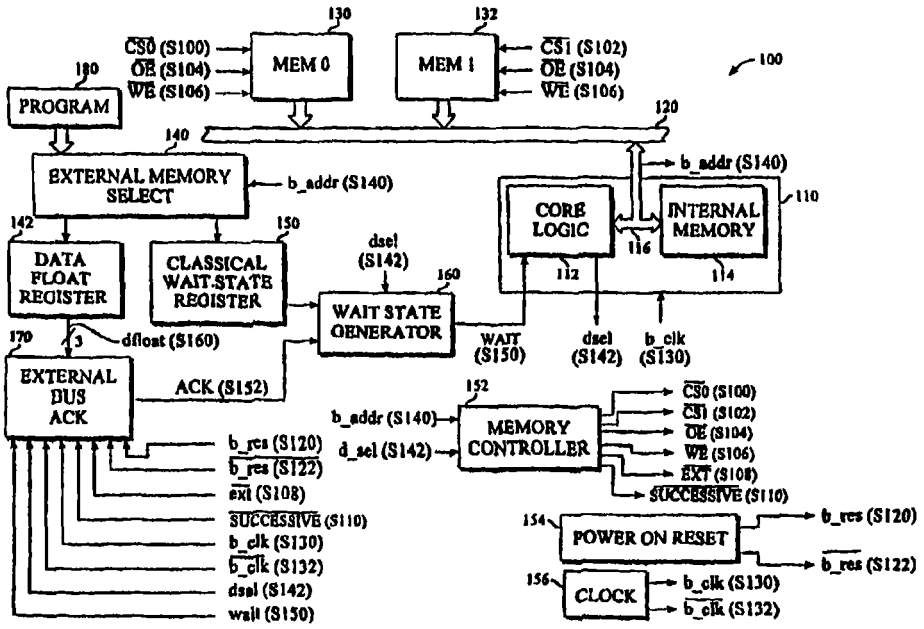
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(54) Title: MICROPROCESSING DEVICE HAVING PROGRAMMABLE WAIT STATES



(57) Abstract

The present invention deals with the control of a data bus (120) by a microcontroller (110), taking into account the fact that memory output drivers require a finite amount of time to electrically release the bus after an output operation. Each memory (130, 132) has an associated wait state number for selectively placing the microcontroller (110) in a wait state of variable length subsequent to a read operation and prior to the next I/O operation.



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