

MEMORY CELL AND MANUFACTURING METHOD THEREOF, AND MEMORY AND MANUFACTURING METHOD THEREOF

ABSTRACT

The present disclosure provides a memory cell and a manufacturing method thereof, and a memory and a manufacturing method thereof, and relates to the technical field of semiconductors. The memory cell includes a first dielectric layer and a second dielectric layer that are stacked. A first transistor is disposed in the first dielectric layer. A second transistor is disposed in the second dielectric layer. The first dielectric layer is connected to the second dielectric layer by using a connecting wire. In the present disclosure, a parasitic capacitance in the first transistor or the second transistor is used as a memory element to replace the capacitor in the related art, such that the volume occupied by the memory cells can be reduced, to ensure that the memory cells are developed in an integration direction. In addition, the first transistor and the second transistor are both metal-oxide thin-film transistors, such that the memory can have longer retention time of charge, to improve the performance of the memory while decreasing the volume of the memory.

FIG. 2