RADIO FREQUENCY SWITCH CONTROL CIRCUITRY

BACKGROUND

Field

[0001] Embodiments of the invention relate to electronic systems, and in particular, to radio frequency (RF) communication systems.

Description of the Related Technology

[0002] Radio frequency (RF) communication systems can be used for transmitting and/or receiving signals of a wide range of frequencies. For example, an RF communication system can be used to wirelessly communicate RF signals in a frequency range of about 30 kHz to 300 GHz, such as in the range of about 400 MHz to about 7.125 GHz for Frequency Range 1 (FR1) of the Fifth Generation (5G) communication standard or in the range of about 24.250 GHz to about 71.000 GHz for Frequency Range 2 (FR2) of the 5G communication standard.

[0003] Examples of RF communication systems include, but are not limited to, mobile phones, tablets, base stations, network access points, customer-premises equipment (CPE), laptops, and wearable electronics.

SUMMARY

[0004] In certain aspect, the present disclosure relates to a mobile device. The mobile device includes a power management system including a positive charge pump configured to generate a positive charge pump voltage, a negative charge pump configured to generate a negative charge pump voltage, and a voltage regulator configured to generate a regulated voltage. The mobile device further includes a front end system including a radio frequency switch controlled by a first switch control signal, and a level shifter operable to level shift a first switch enable signal to generate the first switch control signal at a first output. The level shifter includes a first level-shifting n-type transistor and a first cascode n-type transistor in series between the negative charge pump voltage and the first output, a first level-shifting p-type transistor and a first cascode p-type transistor in series between the positive charge pump voltage and the first output, and a second cascode p-type transistor between the regulated

voltage and a gate of the first level-shifting n-type transistor and controlled by the first switch enable signal.

[0005] In some examples, the level shifter is further operable to level shift a second switch enable signal to generate a second switch control signal at a second output, the second switch enable signal of complementary polarity to the first switch enable signal. According to a number of examples, the level shifter further includes a second level shifting n-type transistor in series with the second cascode p-type transistor between the regulated voltage and the negative charge pump voltage, a third cascode p-type transistor, and a third level shifting n-type transistor in series with the third cascode p-type transistor between the regulated voltage and the negative charge pump voltage. In accordance with various examples, the level shifter further includes a fourth level shifting n-type transistor and a second cascode n-type transistor in series between the second output and the negative charge pump voltage, and a second level shifting p-type transistor and a fourth cascode p-type transistor in series between the positive charge pump voltage and the second output.

[0006] In several examples, the front end system further includes a power amplifier configured to provide a radio frequency signal to the radio frequency switch.

[0007] In some examples, the power management system further includes a charge pump clock generator including a multi-phase oscillator configured to generate a plurality of oscillator clock signals, and a clock phase logic and combining circuit configured to process the plurality of oscillator clock signals to generate a first clock signal of higher frequency than an oscillation frequency of the multi-phase oscillator, the first clock signal operable to control at least one of the positive charge pump or the negative charge pump. According to a number of examples, the clock phase logic and combining circuit is further configured to generate a second clock signal offset in phase from the first clock signal, the first clock signal operable to control the positive charge pump and the second clock signal operable to control the negative charge pump.

[0008] In certain aspect, the present disclosure relates to a radio frequency switch system. The radio frequency switch system includes a radio frequency switch configured to receive a radio frequency signal and controlled by a first switch control signal, a positive charge pump configured to generate a positive charge pump voltage, a negative charge pump configured to generate a negative charge pump voltage, a voltage regulator configured

to generate a regulated voltage, and a level shifter operable to level shift a first switch enable signal to generate the first switch control signal at a first output. The level shifter includes a first level-shifting n-type transistor and a first cascode n-type transistor in series between the negative charge pump voltage and the first output, a first level-shifting p-type transistor and a first cascode p-type transistor in series between the positive charge pump voltage and the first output, and a second cascode p-type transistor between the regulated voltage and a gate of the first level-shifting n-type transistor and controlled by the first switch enable signal.

[0009] In some examples, the level shifter is further operable to level shift a second switch enable signal to generate a second switch control signal at a second output, the second switch enable signal of complementary polarity to the first switch enable signal. According to a number of examples, the level shifter further includes a second level shifting n-type transistor in series with the second cascode p-type transistor between the regulated voltage and the negative charge pump voltage, a third cascode p-type transistor, and a third level shifting n-type transistor in series with the third cascode p-type transistor between the regulated voltage and the negative charge pump voltage. In accordance with several examples, the level shifter further includes a fourth level shifting n-type transistor and a second cascode n-type transistor in series between the negative charge pump voltage and the second output, and a second level shifting p-type transistor and a fourth cascode p-type transistor in series between the positive charge pump voltage and the second output. According to various examples, the radio frequency switch system further includes a first enable level shifting circuit configured to level shift the first switch enable signal to generate a first level shifted switch enable signal that controls a gate of the second level shifting p-type transistor, and a second enable level shifting circuit configured to level shift the second switch enable signal to generate a second level shifted switch enable signal that controls a gate of the first level shifting p-type transistor. In accordance with a number of examples, a gate of the first cascode p-type transistor and a gate of the fourth cascode p-type transistor are connected to a ground voltage. According to several examples, a gate of the second level shifting n-type transistor and a gate of the fourth level shifting n-type transistor are connected to a drain of the third level shifting n-type transistor, and the gate of the first level shifting n-type transistor and a gate of the third level shifting n-type transistor are connected to a drain of the second level shifting n-type transistor. In accordance with various examples, the radio

frequency switch includes a series transistor switch electrically connected between an input terminal and an output terminal and controlled by the first switch control signal, and a shunt transistor switch electrically connected between the input terminal and a ground voltage and controlled by the second switch control signal.

[0010] In several examples, the radio frequency switch system further includes a charge pump clock generator including a multi-phase oscillator configured to generate a plurality of oscillator clock signals, and a clock phase logic and combining circuit configured to process the plurality of oscillator clock signals to generate a first clock signal of higher frequency than an oscillation frequency of the multi-phase oscillator, the first clock signal operable to control at least one of the positive charge pump or the negative charge pump. According to a number of examples, the clock phase logic and combining circuit is further configured to generate a second clock signal offset in phase from the first clock signal, the first clock signal operable to control the positive charge pump and the second clock signal operable to control the negative charge pump.

[0011] In various examples, the voltage regulator is a low dropout regulator.

[0012] In certain aspect, the present disclosure relates to a level shifter for a radio frequency switch. The level shifter includes a first level-shifting n-type transistor, a first cascode n-type transistor in series with the first level-shifting n-type transistor between a negative charge pump voltage and a first output that provides a first switch control signal, a first level-shifting p-type transistor, a first cascode p-type transistor in series with the first level-shifting p-type transistor between a positive charge pump voltage and the first output, and a second cascode p-type transistor between a regulated voltage and a gate of the first level-shifting n-type transistor and controlled by a first switch enable signal.

[0013] In several examples, the level shifter further includes a second level shifting n-type transistor in series with the second cascode p-type transistor between the regulated voltage and the negative charge pump voltage, a third cascode p-type transistor, and a third level shifting n-type transistor in series with the third cascode p-type transistor between the regulated voltage and the negative charge pump voltage. According to a number of examples, the level shifter further includes a fourth level shifting n-type transistor and a second cascode n-type transistor in series between a second output and the negative charge pump voltage, and a second level shifting p-type transistor and a fourth cascode p-type

transistor in series between the positive charge pump voltage and the second output. In accordance with various examples, the level shifter further includes a first enable level shifting circuit configured to level shift the first switch enable signal to generate a first level shifted switch enable signal that controls a gate of the second level shifting p-type transistor, and a second enable level shifting circuit configured to level shift a second switch enable signal to generate a second level shifted switch enable signal that controls a gate of the first level shifting p-type transistor. According to several examples, a gate of the first cascode p-type transistor and a gate of the fourth cascode p-type transistor are connected to a ground voltage. In accordance with a number of examples, a gate of the second level shifting n-type transistor and a gate of the fourth level shifting n-type transistor are connected to a drain of the third level shifting n-type transistor, and the gate of the first level shifting n-type transistor and a gate of the third level shifting n-type transistor are connected to a drain of the second level shifting n-type transistor.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] Figure 1 is a schematic diagram of one example of a communication network.

[0015] Figure 2A is a schematic diagram of one example of a communication link using carrier aggregation.

[0016] Figure 2B illustrates various examples of uplink carrier aggregation for the communication link of Figure 2A.

[0017] Figure 2C illustrates various examples of downlink carrier aggregation for the communication link of Figure 2A.

[0018] Figure 3A is a schematic diagram of one example of a downlink channel using multi-input and multi-output (MIMO) communications.

[0019] Figure 3B is schematic diagram of one example of an uplink channel using MIMO communications.

[0020] Figure 3C is schematic diagram of another example of an uplink channel using MIMO communications.

[0021] Figure 4 is a schematic block diagram of one embodiment of a power amplifier system.