A WAFER LEVEL PACKAGE AND A METHOD OF FORMING THE SAME

ABSTRACT

According to embodiments of the present invention, a wafer level package is provided. The wafer level package includes at least one chip comprising at least one electronic component, and at least one connecting chip comprising at least one through-silicon via, wherein the at least one through-silicon via is electrically coupled to the at least one chip. Further embodiments relate to a method of forming the wafer level package.

Figure 3