Description

This invention relates to an apparatus for generating a skew corrected master clock signal MCS for use in a digital television receiver.

In a digital TV receiver, a broadcast analog color video signal is applied to a conventional receiving antenna. The signal received by the antenna is processed by an analog tuner and intermediate frequency (IF) circuitry. A baseband composite video signal CVS from the IF circuitry is applied to an analog-to-digital (A/D) converter. The A/D converter develops binary or digital representations of the analog composite video signal CVS in response to a sampling or master clock signal MCS. The binary samples are processed in digital circuits to appropriately condition the luminance Y (luma) and chrominance C (chroma) components of the composite video signal CVS for application to the matrixing circuitry of the TV receiver. The Red (R), Green (G) and Blue (B) signals developed by the matrix circuits are converted back to the analog format for application to the kinescope.

For chroma demodulation, it is advantageous to set the frequency of the sampling clock signal MCS at four (4) times the color subcarrier rate F_{sc}, and to phase lock the 4 F_{sc} clock signal to the color burst signal BS incorporated in the incoming composite video signal CVS. Sampling the chrominance signal C using a 4 F_{sc} burst locked clock (BLC) produces the following sample sequence:
-(B-Y),-(R-Y),(B-Y),(R-Y),-(B-Y) and so on. Demodulation may be accomplished by merely demultiplexing the sample stream into separate (R-Y) and (B-Y) data streams.

However, for memory based features (e.g., pix-in-pix, freeze picture, zoom, recursive filtering, etc.), it is desirable to process the video signal with a line locked clock (LLC). A line locked clock produces a fixed integer number (e.g., 910) of sampling points per (horizontal) line. This simplifies memory based video features processing (e.g., line, field or frame memories), because the respective samples are vertically aligned (i.e., TV raster is orthogonally sampled).

For a standard NTSC video signal (e.g., broadcast TV signal), a sampling clock frequency, which is an even integer multiple of the color subcarrier frequency F_{sc}, contains a fixed integer number of clock pulses in every horizontal line period. The color subcarrier frequency F_{sc} is established at 455/2 times the horizontal line frequency F_H (i.e., $F_{sc}=(455/2) \times F_H$) in a standard NTSC TV Signal. A sampling clock frequency F_{MCS} of 4 F_{sc} has exactly 910 clock periods (4 x 455/2) in every horizontal line period. For a standard NTSC video signal, a clock signal may be concurrently burst locked and line locked, thereby facilitating both chroma demodulation and memory based applications (e.g., zoom).

However, not all NTSC compatible TV signals conform precisely to the NTSC broadcast standard format. For example, signals produced by a video cassette recorder (VCR) have varying horizontal line periods in the reproduced signal. This results in a variation in the number of clock pulses developed per horizontal line (e.g., 909.9, 910, 910.1, etc.). In general, for non-standard TV signals, it is not possible that a clock signal be simultaneously burst locked and line locked.

Two previously known approaches for processing non-standard TV signals in the digital domain employ either a burst locked clock or a line locked clock. The use of a burst locked clock simplifies chroma demodulation. However, a burst locked clock produces a variation in the number of clock pulses per horizontal line, and, therefore, causes a line-to-line variation in the phase of the clock signal relative to the horizontal synchronizing component. The line-to-line phase variation of the clock signal relative to the horizontal sync signal causes misalignment of the respective picture elements (pixels) from successive lines of the TV raster, thereby requiring additional processing for memory-based features.

In order to compensate for the line-to-line misalignment of the pixels before they are written into the memory in a burst locked clock system, the input signal samples are time shifted or skew corrected for the phase differences between the incoming horizontal sync pulses IHSP's and the sampling clock pulses MCSP's. Additionally, the signal samples read out from the memory are corrected for skew errors prior to their application to the RGB matrix of the TV receiver. U. S. Patent No. US-A-4,638,360, entitled "TIMING CORRECTION FOR A PICTURE-IN-PICTURE TELEVISION SYSTEM", describes illustrative circuitry for correcting timebase errors in the incoming and outgoing signals in a memory-based video signal processing system, which uses a burst locked clock.

Alternately, one may use a line locked clock for sampling non-standard TV signals. Although this simplifies video features processing (e.g., pix-in-pix), it complicates the chroma demodulation operation when the TV signal is non-standard. Refer to a paper presented by Tom Nillesen, entitled "LINE LOCKED DIGITAL COLOUR DECODING", at the International Conference on Consumer Electronics in June, 1985 in Chicago for details of a chroma demodulation apparatus that operates in a line locked clock system.

In accordance with this invention, an apparatus is disclosed for generating a skew corrected master clock signal MCS. The apparatus includes an oscillator for providing a fixed frequency signal FFOS having

a frequency which is a fixed integer multiple K of the desired nominal frequency (e.g., 4 F_{sc}) of the skew corrected master clock signal MCS. A frequency divide-by-K circuit coupled for receiving the fixed frequency oscillator signal FFOS generates the skew-corrected master clock signal MCS, which is reset at the beginning of every horizontal line.

The skew corrected master clock signal MCS is not locked to the burst phase. Furthermore, the skew corrected master clock does not provide a fixed integer number of clock pulses per horizontal line, and, therefore, is not line locked. However, the phase of the skew corrected master clock signal MCS is reset at the beginning of every horizontal line. Once the phase of the skew corrected master clock signal MCS is reset, its frequency is fixed (e.g., 4 F_{sc}) until the start of the next horizontal line.

In accordance with a first aspect of the invention, the frequency divide-by-K circuit comprises a divide-by-m circuit connected in series with a flip-flop, with said divide-by-m circuit reset by a first control signal FCS once every horizontal line, the apparatus further including means for preventing the output of said flip-flop from changing while said divide-by-m circuit is reset.

In accordance with a second aspect of the present invention, the state of the frequency divide-by-K circuit is captured and saved (for use, for example in a chroma demodulation apparatus) just before it is reset.

IN THE DRAWINGS:

FIGURE 1 is a block diagram of an apparatus for generating a skew-corrected master clock signal MCS, and an accompanying skew error signal SES, in accordance with the present invention;

FIGURE 2 is a logic schematic of an apparatus for generating a pair of control signals FCS and SCS for use in the FIGURE 1 clock signal generating apparatus;

FIGURE 3 illustrates signal waveforms useful in understanding the operation of the FIGURE 2 control signal generating apparatus;

FIGURES 4 and 5 represent signal waveforms useful in describing the function of the FIGURE 1 clock signal generating apparatus;

FIGURE 6 is a block diagram of a chroma demodulation apparatus for use with the skew corrected clock signal MCS; and

FIGURE 7 is a partial block diagram of an apparatus for generating a new line signal NLS for use in the FIGURE 6 chroma demodulation apparatus.

In the DRAWINGS, the lines interconnecting various blocks represent either single conductor connections carrying analog signals or multi-conductor buses carrying multi-bit parallel digital signals, as the case may be.

It will be readily appreciated by those skilled in the video signal processing art that many of the functions described hereinbelow may be practiced in either digital or analog domain.

It is assumed that the incoming video signal nominally conforms to the NTSC standard format. Examples of signals conforming nominally to the NTSC standard format are video signals produced by a video cassette recorder or a video disc player (hereinafter, non-standard video signals). It is further assumed that the desired, nominal clock frequency F_{MCS} is four (4) times the color subcarrier frequency F_{sc}.

FIGURE 1 depicts an apparatus 20 for generating a skew corrected master clock signal MCS in accordance with the principles of the present invention. The skew corrected master clock signal MCS is utilized in the FIGURE 6 chroma demodulation apparatus 200 in the manner described later.

The FIGURE 1 clock generating apparatus 20 includes a free running oscillator 22 for providing an asynchronous fixed frequency oscillator signal FFOS. The frequency F_{FFOS} of the free running oscillator 22 is established at a fixed integer multiple K (e.g., 32) of the desired nominal frequency (e.g., 4 F_{sc}) of the skew corrected clock signal MCS.

A frequency divide-by-K circuit 30 (hereinafter, divider) is coupled to the output terminal 24 of the asynchronous oscillator 22 for generating the skew corrected master clock signal MCS at its output terminal 32. The phase of the clock signal MCS is reset at the start of every line following the occurrence of a horizontal sync signal pulse IHSSP in the manner explained below.

An advantage of the subject invention is that a free running, fixed frequency oscillator 22 is used instead of a line locked, voltage controlled oscillator (VCO). Another advantage is that the master clock signal MCS is reset every horizontal line, whereby the timing of the pixels is consistent from line to line. This facilitates implementation of memory based applications (e.g., recursive filtering, zoom, pix-in-pix, freeze, etc.).

The choice of the oscillator frequency is determined by the timing resolution required for the picture elements. It is advantageous to establish the multiple K (F_{FFOS}/4 F_{sc}) equal to an integer power or an integer

multiple of two (e.g., 128) to simplify the design of the divider 30. A 1.832727 GHz oscillator frequency F_{FFOS}, for example, is 128 times the desired nominal frequency 14.31818 MHz (4 F_{sc}) of the master clock signal MCS. It results in 0.546 nsec of timing resolution for the television raster.

The divider 30 comprises a divide-by-m circuit 40 (where m is a fixed integer) connected in series with a JK flip-flop 50. When m is a power of 2 (e.g., 16), the divide-by-m circuit 40 can be implemented with a plurality of toggle flip-flops 42, 44 ... and 48 connected in a ripple configuration in the manner shown in FIGURE 1. The toggle flip-flops 42-48 are reset once every horizontal line in response to a first control or timing signal FCS.

FIGURE 2 depicts an apparatus 100 for generating the first control signal FCS in response to the fixed frequency oscillator signal FFOS, and a particular edge 102 (e.g., the leading edge) of an incoming horizontal sync signal pulse IHSSP. The horizontal sync signal IHSS applied to the control signal generating apparatus 100 is a continuous-time analog signal. The horizontal sync signal IHSS may be derived from the conventional horizontal phase locked loop circuits of the TV receiver.

The control signal generating apparatus 100 includes a plurality of D flip-flops 104, 106 and 108, and a pair of OR gates 110 and 112. The operation of the control signal generating apparatus 100 will be explained in conjunction with the waveforms illustrated in FIGURE 3.

The fixed frequency oscillator signal FFOS (waveform 3.a) is applied to the clock input terminals of the flip-flops 104-108. The leading edge 102 (waveform 3.b) of an incoming horizontal sync signal pulse IHSSP is coupled to the data input terminal D_1 of the first flip-flop 104. The Q_1 and $\overline{Q}_1$ outputs (waveforms 3.c and 3.d) of the first flip-flop 104 are applied to an input terminal of the OR gate 112 and the data input terminal D_2 of the second flip-flop 106, respectively. The Q_2 and $\overline{Q}_2$ outputs (waveforms 3.e and 3.f) are coupled to the data input terminal D_3 of the third flip-flop 108 and an input terminal of the OR gate 110, respectively. The Q_3 output (waveform 3.g) of the third flip-flop 108 is applied to the respective input terminals of the OR gates 110 and 112. The first and second control or timing signals FCS and SCS (waveforms 3.h and 3.i) are generated at the output terminals 114 and 116 of the OR gates 110 and 112, respectively. The waveform 3.j shows the inverted value $\overline{SCS}$ of the second control signal SCS.

As will be seen from the waveform 3.h, the first control signal FCS extends from the second rising edge 122 of the fixed frequency oscillator signal FFOS (following the occurrence of the leading edge 102 of an incoming horizontal sync signal pulse IHSSP) and the third rising edge 124 thereof. The second control signal SCS extends from the first rising edge 120 to the third rising edge 124 of the fixed frequency oscillator signal FFOS in the manner illustrated in the waveform 3.i. The leading edge 126 of the first control signal pulse FCSP occurs after the leading edge 128 of the associated second control signal pulse SCSP.

As previously indicated, the divider 30 consists of a divide-by-m circuit 40 and a JK flip-flip 50. The output Q_4 of the toggle flip-flop 48 of the divide-by-m circuit 40 is applied to the clock input terminal of the JK flip-flop 50 via an AND gate 66. The second control signal SCS is coupled to the J and K input terminals of the flip-flop 50. The application of the second control signal SCS to the J and K input terminals of the flip-flop 50 prevents a change in its Q output (i.e., MCS signal) while the divide-by-m circuit 40 is being reset once every line in response to the first control signal FCS.

Pursuant to another feature of the present invention, the clock signal generating apparatus 20 further includes a circuit 60, shown in FIGURE 1, for aligning the next predetermined transition (i.e., rising or falling) of each skew corrected clock signal pulse MCSP (occurring after every incoming horizontal sync signal pulse IHSSP), regardless of the output state Q_5 of the JK flip-flop 50 during the reset operation. The function of the aligning circuit 60 is explained below with the help of the waveforms in FIGURES 4 and 5.

The aligning circuit 60 includes a JK flip-flop 62, an OR gate 64 and an AND gate 66. The J and K input terminals of the flip-flop 62 are respectively biased at a logical one state (+5V) and a logical zero state (ground). The clock input terminal of the flip-flop 62 is coupled for receiving the output signal Q_4 of the toggle flip-flop 48.

The OR gate 64 has input terminals coupled for receiving the second control signal SCS and the output signal Q_5/MCS of the JK flip-flop 50, and has an output terminal coupled to the reset terminal of the JK flip-flop 62. The AND gate 66 has input terminals coupled for receiving the output signal Q_4 of the toggle flip-flop 48 and the output signal Q_5'' of the JK flip-flop 62. The output of the AND gate 66 is applied to the clock input terminal of the JK flip-flop 50.

FIGURE 4 shows a situation where the control signals FCS and SCS (waveforms 4.b and 4.c) occur while the clock signal Q_5/MCS (waveform 4.d) is low. FIGURE 5 depicts the situation where the control signals FCS and SCS (waveforms 5.b and 5.c) occur while the clock signal Q_5/MCS (waveform 5.d) is high. It will be seen that the very first rising edges 80 and 82 of the clock signal MCS occur after a fixed time interval "δ" following the termination of the first control signal pulses FCSP's 70 and 72, respectively. This is so regardless of whether the clock signal MCS is low or high at the time of the occurrence of the control

or timing signals FCS and SCS.

The waveform 4.a depicts the output signal Q_4 of the divide-by-m circuit 40. The toggle flip-flops 42-48 of the divide-by-m circuit 40 are reset by the first control signal FCS (waveform 4.b). Once the reset pulse FCSP 70 is removed, the output Q_4 of the divide-by-m circuit 40 follows the regular pattern shown by the waveform 4.a (i.e., one falling edge 84 of the Q_4 signal for every m cycles of the FFOS signal).

The reset pulse RP (waveform 4.e) causes the output signal Q_5'' (waveform 4.f) of the JK flip-flop 62 to go low. The signal Q_5'' remains low until the occurrence of the first negative going edge 84 of the signal Q_4 (waveform 4.a) applied to the clock input terminal of the flip-flop 62, at which time the signal Q_5'' goes high.

The signal Q_4'' (waveform 4.g) at the output of the AND gate 66 follows the input signal Q_4 (waveform 4.a) when the other input signal Q_5'' (waveform 4.f) from the JK flip-flop 62 is high. When the J and K input terminals of the flip-flop 50 are low (i.e., SCS is low), its output Q_5 remains low. When the J and K input terminals of the flip-flop 50 are high (i.e. SCS is high), every negative going edge of the clock input signal Q_4'' causes the flip-flop 50 to change its output state Q_5. The output (waveform 4.d) of the JK flip-flop 50 is the skew corrected clock signal MCS.

As previously indicated, the waveforms in FIGURE 5 illustrate a situation where the control signals FCS and SCS (waveforms 5.b and 5.c) occur while the clock signal Q_5/MCS (waveform 5.d) is high. The waveforms 5.a, 5.b and 5.c depicting the signals Q_4, FCS and SCS are the same as the respective waveforms 4.a, 4.b and 4.c in FIGURE 4.

The output Q_5'' (waveform 5.f) of the JK flip-flop 62 remains high, because the flip-flop 62 is not reset. The output Q_4'' (waveform 5.g) of the AND gate 66 follows the output signal Q_4 (waveform 5.a) of the divide-by-m circuit 40. Since the J and K inputs of the flip-flop 50 are high (i.e., SCS is high), every falling edge of the clock input signal Q_4'' (waveform 5.g) triggers the JK flip-flop 50. The waveform 5.d depicts the output MCS of the JK flip-flop 50. It will be noted that the very first rising edge 82 of the clock signal MCS occurs the same time interval "δ" after the divide-by-m circuit 40 is reset in response to the first control signal FCS.

The clock generating apparatus 20 further includes means 150 coupled to the divider 30 for capturing and saving the current state SES thereof before the divider is reset every horizontal line in response to the first control signal FCS. The state signal SES (which represents the divider count at the time the divider 30 is reset) is indicative of the skew or phase error of the clock signal MCS relative to the associated horizontal sync pulse IHSSP at the start of each line. The state capturing means 150 comprises of a plurality of D flip-flops 152, 154, ... 158 and 160 having their D input terminals coupled for receiving the respective output states Q_1, Q_2 ... Q_4 and $\overline{Q_5}$ of the divider flip-flops 42, 44, ... 48 and 50. The complement $\overline{SCS}$ (waveform 3.j) of the second control signal SCS is applied to all of the clock input terminals of the state capturing flip-flops 152-160.

The current state SES of the divider flip-flops 42-50, indicative of the skew or phase error, is latched into the respective flip-flops 152-160 in response to the $\overline{SCS}$ signal. From FIGURE 3, it will be seen that the leading edge 128 of the second control signal pulse SCSP (waveform 3.i) occurs prior to the leading edge 126 of the first control signal pulse FCSP (waveform 3.h). This allows the state capturing means 150 to save the current state SES of the divider 30 before it is reset by the first control signal FCS.

The chroma demodulation apparatus 200 utilizes the skew corrected clock signal MCS and the state signal SES (indicative of the skew error) in the manner illustrated in FIGURE 6. The FIGURE 6 chroma demodulation apparatus is the subject matter of US patent application 032,829 (US-A-4 736 237), to which corresponds a British application filed contemporaneously herewith (RCA 84248).

The incoming composite video signal CVS is applied to the input terminal 202 of an analog-to-digital (A/D) converter 210. The A/D converter 210 generates digital representations CVS′ of the incoming video signal CVS at a rate determined by the skew corrected clock signal MCS.

The digital samples CVS′ are applied to a pair of multipliers 220 and 230, where they are multiplied by the respective cosine and sine values of the phase angle ϕ_{sc} of a burst locked color subcarrier signal, where $\phi_{sc} = \omega_{sc} \cdot t$ or $2\pi \cdot F_{sc} \cdot t$. The output FMO and SMO of the first and second multipliers 220 and 230 can be represented as follows:

$$FMO = (B\text{-}Y) + \text{double frequency } (2F_{sc}) \text{ components} \quad 1$$

$$SMO = (R\text{-}Y) + \text{double frequency } (2F_{sc}) \text{ components} \quad 2$$

In the above equations, (B-Y) and (R-Y) are color difference signals, and the double frequency components are signal components having twice the color subcarrier frequency F_{sc}. A pair of lowpass filters 250 and 260 are coupled to the respective multipliers 220 and 230 for eliminating undesirable double

frequency (2 F_{sc}) components from the outputs thereof.

The sine and cosine values applied to the multipliers 220 and 230 are generated by a random access, read only memory (ROM) 240 in response to the instantaneous phase ϕ_{sc} of an internally-generated signal phase-locked to the color subcarrier signal. The description of how the phase angle information ϕ_{sc} is generated is given later.

The chroma demodulation apparatus 200 includes a circuit 300 for generating the instantaneous phase angle ϕ_{sc} of a burst locked color subcarrier representative signal. The circuit 300 comprises a discrete time oscillator (DTO) 310, means 320 for accounting for once-a-line discontinuities in the skew corrected clock signal MCS, and means 330 for supplying the burst phase error information. The DTO 310 includes a delay element 312 and an adder 314. The delay element 312 consists of a plurality (p) of D flip-flops, which are clocked with the master clock signal MCS. At each clock period, the adder 314 adds to the p-bit previous sum (at a first input terminal 316) a (p-1) bit increment (at a second input terminal 318). Only p bits of the adder output are latched by the D flip-flops, thereby forming a modulo (2^p) accumulator.

The increment at the terminal 318 consists of the sum of:

- a (p-1) bit value NCSS on terminal 340 representative of the nominal color subcarrier frequency F_{sc} - (i.e., 3.58 MHz in the NTSC format),
- a (p-1) bit value NSES on terminal 322 representative of the normalized value of the q-bit state or skew error signal SES, once every line, and
- (p-12) active bit value PES on terminal 332 representative of the phase error $\Delta\phi_{sc}$ between the internally-generated, color subcarrier representative signal ϕ_{sc} and the burst signal BS included in the incoming composite video signal CVS.

The value of p is selected so as to obtain the desired degree of resolution in the production of the color subcarrier representative signal ϕ_{sc}. The relationship between the resolution r in HZ. (e.g., 30 HZ.), the nominal clock frequency F_{MCS} (e.g., 14.3 MHz in the NTSC format) and the number of bits p is given below:

$$r = F_{MCS}/2^p.$$

In this particular embodiment, p is 20 bits.

An adder 350 adds the phase error signal PES on the terminal 332 to the nominal value NCSS of the color subcarrier frequency on the terminal 340. Another adder 360 adds the normalized value of the state or skew error signal NSES on the terminal 322 to the output of the adder 350, once every horizontal line.

Consider the following illustrative situation:

- p = 8 bits
- q = 5 bits
- Phase Error Signal PES = 0
- Normalized State or Skew Error Signal NSES = 0
- Nominal frequency of the master clock signal MCS is 4 F_{sc}
- Nominal digital value representative of the color subcarrier signal is given below:

$$\begin{aligned} NCSS &= 2^p/4 \\ &= 2^{p-2} \\ &= 2^6 \\ &= 0100\ 0000 \end{aligned}$$

Under these circumstances, the modulo 2^8 output of adder 314 is incremented by a constant increment 0100 0000 at each clock period. The output sequence is given below:

DTO OUTPUT	
CLOCK NO.	ADDER OUTPUT
1	0000 0000
2	0100 0000
3	1000 0000
4	1100 0000
5	0000 0000
6	0100 0000
7	1000 0000
8	1100 0000
9	0000 0000
:	:
.	.

From the above table, it can be seen that the output of the DTO 310 is a sawtooth type response, which cycles through a set of four values (0000 0000, 0100 0000, 1000 0000 and 1100 0000) at the F_{sc} rate (i.e., one cycle for every 4 clock pulses). In this illustrative example, the DTO output values are established by the NCSS value (i.e. 0100 0000), which represents the nominal value of the color subcarrier signal frequency F_{sc}. As previously indicated, both PES and NSES values are assumed to be zero.

The functional block 320 comprises of a multiplier 324 and an AND gate 326. The multiplier 324 provides a (p-1) bit normalized digital value NSES by multiplying the q-bit skew error signal SES by a normalizing factor NF = $2^{p-q}/4$. Since the normalizing factor NF is an integer power of 2, the multiplication function can be realized by simple bit shifting.

One input of the AND gate 326 is coupled for receiving the p-1 bit normalized skew error signal NSES. The complement $\overline{NLS}$ (4.i and 5.i) of a new line signal NLS is applied to the other input of the AND gate 326. The AND gate 326 provides the normalized skew error signal NSES at its output terminal 322, once every horizontal line, in response to the $\overline{NLS}$ signal. Addition of the normalized skew error signal NSES to the nominal value NCSS of the color subcarrier signal compensates the DTO output ϕ_{sc} for the stretching of clock pulses MCSP's at the start of every horizontal line.

A D flip-flop 370, shown in FIGURE 7, provides the new line signal $\overline{NLS}$. The D input terminal of the flip-flop 370 is biased at a logical one state (+5V). The clock signal MCS and the second control signal SCS are applied to the clock input terminal and the reset terminal of the flip-flop 370, respectively. The waveforms 4.i and 5.i show the $\overline{NLS}$ signal at the output terminal 372 of the flip-flop 370.

The functional block 330 comprises an AND gate 334 and a burst loop filter 336. The AND gate 334 has input terminals coupled for receiving the signal at the terminal 262 and the burst gate signal BGS. The burst gate signal BGS is a logical one during the burst segment of the incoming composite video signal CVS. The AND gate 334 provides, at the output thereof, the output of the lowpass filter 260 when the burst gate signal BS is a logical one. During this interval, the output of the lowpass filter 260 represents the phase error $\Delta\phi_{sc}$ between the internally-generated, color subcarrier representative signal ϕ_{sc} and the burst signal BS included in the incoming composite video signal CVS.

When the internally-generated ϕ_{sc} signal is in phase with the burst signal BS, the output of the lowpass filter 260 is zero. When the ϕ_{sc} signal leads the BS signal, the output of the lowpass filter 260 is negative. On the other hand, when the ϕ_{sc} signal lags the BS signal, the output of the lowpass filter 260 is positive.

The burst loop filter 336 produces a weighted average PES (e.g., $\Sigma\ w_i\ .\Delta\phi_{sc}$) of the output $\Delta\ \phi_{sc}$ of the AND gate 334 over several cycles of the burst signal BS. Addition of a positive or a negative phase error value PES to the nominal value NCSS of the color subcarrier signal, respectively, speeds up or slows down the DTO output frequency in a manner that causes the DTO output ϕ_{sc} to synchronize with the burst signal BS.

The ROM 240 generates sine and cosine function values for the phase angles represented by the ϕ_{sc} values applied to the address input port of the ROM. The relationship between the phase angle of the color subcarrier signal and the ϕ_{sc} input of the ROM 240 is given below:

phase angle = $\phi_{sc}/2^p \times 2\pi$,

where ϕ_{sc} represents a positive number.

In summary, color circuit 300 generates a burst locked color subcarrier representative signal ϕ_{sc} from the non-continuous, skew corrected clock signal MCS for use in the chroma demodulation apparatus 200. The DTO 310 provides a modulo (2^p) output, representative of the burst locked, color subcarrier representative signal ϕ_{sc}. The functional block 320 compensates for the once-a-line discontinuities in the skew corrected clock signal MCS. The functional block 330 corrects for phase errors between the internally generated ϕ_{sc} signal and the color burst signal BS in the incoming composite video signal CVS.

Claims

1. A digital television system for processing digital samples of an incoming composite video signal CVS including periodic horizontal sync signal IHSS disposed between successive horizontal lines of picture information; said system further including an apparatus for generating a skew-corrected master clock signal MCS for producing said digital samples of said composite video signal CVS; said apparatus being characterized by:

   an oscillator (22) for providing an asynchronous fixed frequency signal FFOS having a frequency which is a fixed integer multiple K of the desired nominal frequency of said skew-corrected master clock signal MCS;

   control means (100), responsive to said incoming horizontal sync signal IHSS and said asynchronous, fixed frequency oscillator signal FFOS, for generating a first control signal FCS initiated by a predetermined transition of said oscillator signal FFOS following occurrence of the leading edge of each incoming horizontal sync signal pulse IHSSP; and

   frequency dividing means (30), coupled to receive said fixed frequency oscillator signal and subject to being reset by said first control signal FCS once each horizontal line, for generating said skew-corrected master clock signal wherein said frequency of said asynchronous fixed frequency oscillator signal FFOS is an even integer multiple (K=2m, where m is an integer) of said desired nominal frequency of said skew-corrected master clock signal MCS; said dividing means comprising a divide-by-m circuit (40) responsive to said fixed frequency oscillator signal FFOS and a flip-flop (50) responsive to the output of said divide-by-m circuit, wherein the output of said flip-flop comprises said skew-corrected master clock signal MCS, and wherein said divide-by-m circuit is reset by said first control signal FCS once every horizontal line; said apparatus further including means (112, 116) for preventing the output of said flip-flop from changing while said divide-by-m circuit is reset in response to said first control signal FCS.

2. The apparatus defined in Claim 1 wherein said control means further produces a second control signal SCS, initiated by a transition of said oscillator signal FFOS preceding said predetermined transition and terminated by a transition of said oscillator signal FFOS succeeding said predetermined transition, whereby the leading edges of the pulses defining said first control signal FCS occur between the respective leading and trailing edges of the associated pulses defining said second control signal SCS; wherein said flip-flop has a clock input terminal coupled for receiving the output of said divide-by-m circuit, and said flip-flop is conditioned by said second control signal SCS not to change states while said divide-by-m circuit is reset in response to said first control signal FCS.

3. The apparatus defined in Claim 2 further including:

   a further flip-flop (62) having a reset terminal, and having a clock input terminal coupled fur receiving the output of said divide-by-m circuit; said further flip-flop being arranged to change output states each time a predetermined transition occurs at its clock input terminal;

   an OR gate (64) having the respective input terminals thereof coupled for receiving one of said first and second control signals FCS, SCS and the output signal MCS of said first-mentioned flip-flop, and having the output terminal thereof coupled to the reset terminal of said further flip-flop; and

   an AND gate (66) having the respective input terminals thereof coupled for receiving the output of said further flip-flop and said output of said divide-by-m circuit, and having the output terminal thereof coupled to the clock input terminal of said first-mentioned flip-flop.

phase angle = $\phi_{sc}/2^p \times 2\pi$,

where ϕ_{sc} represents a positive number.

In summary, color circuit 300 generates a burst locked color subcarrier representative signal ϕ_{sc} from the non-continuous, skew corrected clock signal MCS for use in the chroma demodulation apparatus 200. The DTO 310 provides a modulo (2^p) output, representative of the burst locked, color subcarrier representative signal ϕ_{sc}. The functional block 320 compensates for the once-a-line discontinuities in the skew corrected clock signal MCS. The functional block 330 corrects for phase errors between the internally generated ϕ_{sc} signal and the color burst signal BS in the incoming composite video signal CVS.

Claims

1. A digital television system for processing digital samples of an incoming composite video signal CVS including periodic horizontal sync signal IHSS disposed between successive horizontal lines of picture information; said system further including an apparatus for generating a skew-corrected master clock signal MCS for producing said digital samples of said composite video signal CVS; said apparatus being characterized by:

   an oscillator (22) for providing an asynchronous fixed frequency signal FFOS having a frequency which is a fixed integer multiple K of the desired nominal frequency of said skew-corrected master clock signal MCS;

   control means (100), responsive to said incoming horizontal sync signal IHSS and said asynchronous, fixed frequency oscillator signal FFOS, for generating a first control signal FCS initiated by a predetermined transition of said oscillator signal FFOS following occurrence of the leading edge of each incoming horizontal sync signal pulse IHSSP; and

   frequency dividing means (30), coupled to receive said fixed frequency oscillator signal and subject to being reset by said first control signal FCS once each horizontal line, for generating said skew-corrected master clock signal wherein said frequency of said asynchronous fixed frequency oscillator signal FFOS is an even integer multiple (K=2m, where m is an integer) of said desired nominal frequency of said skew-corrected master clock signal MCS; said dividing means comprising a divide-by-m circuit (40) responsive to said fixed frequency oscillator signal FFOS and a flip-flop (50) responsive to the output of said divide-by-m circuit, wherein the output of said flip-flop comprises said skew-corrected master clock signal MCS, and wherein said divide-by-m circuit is reset by said first control signal FCS once every horizontal line; said apparatus further including means (112, 116) for preventing the output of said flip-flop from changing while said divide-by-m circuit is reset in response to said first control signal FCS.

2. The apparatus defined in Claim 1 wherein said control means further produces a second control signal SCS, initiated by a transition of said oscillator signal FFOS preceding said predetermined transition and terminated by a transition of said oscillator signal FFOS succeeding said predetermined transition, whereby the leading edges of the pulses defining said first control signal FCS occur between the respective leading and trailing edges of the associated pulses defining said second control signal SCS; wherein said flip-flop has a clock input terminal coupled for receiving the output of said divide-by-m circuit, and said flip-flop is conditioned by said second control signal SCS not to change states while said divide-by-m circuit is reset in response to said first control signal FCS.

3. The apparatus defined in Claim 2 further including:

   a further flip-flop (62) having a reset terminal, and having a clock input terminal coupled fur receiving the output of said divide-by-m circuit; said further flip-flop being arranged to change output states each time a predetermined transition occurs at its clock input terminal;

   an OR gate (64) having the respective input terminals thereof coupled for receiving one of said first and second control signals FCS, SCS and the output signal MCS of said first-mentioned flip-flop, and having the output terminal thereof coupled to the reset terminal of said further flip-flop; and

   an AND gate (66) having the respective input terminals thereof coupled for receiving the output of said further flip-flop and said output of said divide-by-m circuit, and having the output terminal thereof coupled to the clock input terminal of said first-mentioned flip-flop.

4. The apparatus as defined in Claim 3 wherein said dividing means comprises a plurality of divider stages (42, 44...48, 50) , said apparatus further including means (150) for latching the present state of said divider stages prior to said dividing means being reset in response to said first control signal FCS; said latching means comprises a plurality of flip-flops (152, 154...158, 160) having respective data input terminals coupled for receiving the respective bits indicative of the present state of said divider stages, and their clock input terminals coupled for receiving said second control signal SCS, whereby the present state of said divider is latched by said flip-flops upon the occurrence of every second control signal pulse SCSP.

Patentansprüche

1. Digitales Fernsehsystem zur Verarbeitung digitaler Abtastungen eines ankommenden Videosignalgemisches CVS, das ein periodisches Horizontal-Synchronsignal IHSS zwischen aufeinanderfolgenden horizontalen Zeilen einer Bildinformation enthält; wobei das System ferner eine Vorrichtung zur Erzeugung eines verzerrungskorrigierten Haupt-Taktsignals MCS enthält, um die digitalen Abtastungen des Videosignalgemisches CVS zu erzeugen, wobei die Vorrichtung gekennzeichnet ist durch:

einen Oszillator (22) zur Erzeugung eines asynchronen Signals FFOS mit fester Frequenz, die ein festes ganzzahliges Vielfaches K der gewünschten nominellen Frequenz des verzerrungskorrigierten Haupt-Taktsignals MCS ist;

Steuermittel (100), die auf das ankommende Horizontal-Synchronsignal IHSS und das Oszillatorsignal FFOS mit der festen Frequenz ansprechen, um ein erstes Steuersignal FCS zu erzeugen, das durch einen vorgegebenen Übergang des Oszillatorsignals FFOS ausgelöst wird, der dem Auftreten der Vorderflanke jedes ankommenden Horizontal-Synchronsignalimpulses IHSSP folgt; und

Frequenzteilermittel (30) zum Empfang des Oszillatorsignals mit der festen Frequenz, die durch das erste Steuersignal FCS bei jeder horizontalen Zeile einmal zurückgestellt werden, um das verzerrungskorrigierte Haupt-Taktsignal zu erzeugen, wobei die Frequenz des asynchronen Oszillatorsignals FFOS mit der festen Frequenz ein gerades ganzzahliges Vielfaches (K = 2m, wobei m eine ganze Zahl ist) der gewünschten nominellen Frequenz des verzerrungskorrigierten Haupt-Taktsignals MCS ist, wobei die Teilungsmittel eine m-fach-Teilerschaltung (40), die auf das Oszillatorsignal FFOS mit der festen Frequenz anspricht, und einen Flip-Flop (50) enthalten, der auf den Ausgang der m-fach-Teilerschaltung anspricht, wobei der Ausgang des Flip-Flops das verzerrungskorrigierte Haupt-Taktsignal MCS umfaßt, und wobei die m-fach-Teilerschaltung durch das erste Steuersignal bei jeder horizontalen Zeile einmal zurückgestellt wird; wobei die Vorrichtung ferner Mittel (112, 116) enthält, um eine Änderung des Ausgangs des Flip-Flops zu verhindern, wenn die m-fach-Teilerschaltung in Abhängigkeit von dem ersten Steuersignal FCS zurückgestellt wird.

2. Vorrichtung nach Anspruch 1, bei der die Steuermittel ferner ein zweites Steuersignal SCS erzeugen, das durch einen Übergang des Oszillatorsignals FFOS ausgelöst wird, der dem vorgegebenen Übergang vorausgeht, und das durch einen übergang des Oszillatorsignals FFOS beendet wird, der dem vorgegebenen Übergang folgt, wobei die Vorderflanken der das erste Steuersignal FCS definierenden Impulse zwischen entsprechenden vorderen und hinteren Flanken der zugehörigen, das zweite Steuersignal SCS definierenden Impulse auftreten; wobei der Flip-Flop durch das zweite Steuersignal SCS so konditioniert wird, daß er seinen Zustand während der Rückstellung der m-fach-Teilerschaltung in Abhängigkeit von dem ersten Steuersignal nicht ändert.

3. Vorrichtung nach Anspruch 2, die ferner umfaßt:

einen weiteren Flip-Flop (62) mit einem Rückstellanschluß und einem Takt-Eingangsanschluß zum Empfang des Ausgangs der m-fach-Teilerschaltung, wobei der weitere Flip-Flop so ausgebildet ist, daß er die Ausgangszustände jedesmal ändert, wenn ein vorgegebener Übergang an seiner Takt-Eingangsklemme auftritt;

ein ODER-Tor (64), dessen Eingangsanschlüsse eines der ersten und zweiten Steuersignale FCS, SCS und das Ausgangssignal MCS des ersten Flip-Flops empfangen, und dessen Ausgangsanschluß mit dem Rückstellanschluß des weiteren Flip-Flops verbunden ist; und

ein UND-Tor (66), dessen Eingangsanschluß den Ausgang des weiteren Flip-Flops und den Ausgang der m-fach-Teilerschaltung empfangen, und dessen Ausgangsanschluß mit der Takt-Eingangsklemme des ersten Flip-Flops verbunden ist.

* C L M S *

4. Vorrichtung nach Anspruch 3, bei der die Teilungsmittel eine Vielzahl von Teilungsstufen (42, 44 ... 48, 50) umfassen, wobei die Vorrichtung ferner Mittel (150) enthält, um den gegenwärtigen Zustand der Teilerstufen vor der Rückstellung der Teilungsmittel in Abhängigkeit von dem ersten Steuersignal FCS zu verriegeln; wobei die Verriegelungsmittel eine Vielzahl von Flip-Flops (152, 154 ... 158, 160) enthalten, deren Daten-Eingangsanschlüsse die entsprechenden Bits empfangen, die den gegenwärtigen Zustand der Teilerstufen angeben, und deren Takt-Ausgangsanschlüsse das zweite Steuersignal SCS empfangen, wobei der gegenwärtige Zustand des Teilers durch die Flip-Flops bei Auftreten jedes zweiten Steuersignalimpulses SCSP verriegelt wird.

Revendications

1. Système de télévision numérique pour traiter des échantillons numériques d'un signal vidéo composite (CVS) entrant comprenant un signal de synchro horizontale périodique IHSS disposé entre les lignes horizontales successives de l'information image ; ledit système comprenant, de plus, un dispositif pour générer un signal d'horloge maître MCS corrigé en distorsion pour produire lesdits échantillons numériques dudit signal vidéo composite CVS ; ledit dispositif étant caractérisé par :

   un oscillateur (22) pour fournir un signal de fréquence fixe asynchrone FFOS aynt une fréquence qui est un multiple entier fixé K de la fréquence nominale souhaitée dudit signal d'horloge maitre corrigé en distorsion MCS ;

   un moyen de commande (100), sensible audit signal de synchro horizontale entrant IHSS et audit signal d'oscillateur de fréquence fixe, asynchro FFOS pour générer un premier signal de commande FCS initié par une transition prédéterminée dudit signal d'oscillateur FFOS suivant l'apparition du front avant de chaque impulsion du signal de synchro horizontale entrant IHSSP ; et

   un moyen diviseur de fréquence (30) couplé pour recevoir ledit signal d'oscillateur de fréquence fixe et sujet à être réinitialisé par ledit premier signal de commande FCS une fois à chaque ligne horizontale, pour générer ledit signal d'horloge maitre corrigé en distorsion dans lequel ladite fréquence dudit signal d'oscillateur de fréquence fixe asynchrone FFOS est un multiple entier pair (K = 2m où m est un entier) de ladite fréquence nominale souhaitée dudit signal d'horloge maitre corrigé en distorsion MCS ; ledit moyen diviseur comprenant un circuit de division par m (40) sensible audit signal d'oscillateur de fréquence fixe FFOS et une bascule (50) sensible à la sortie dudit circuit de division par m, dans lequel la sortie de ladite bascule comprend ledit signal d'horloge maitre corrigé en distorsion MCS et dans lequel ledit circuit de division par m est réinitialisé par ledit premier signal de commande FCS une fois à chaque ligne horizontale ; ledit dispositif incluant, de plus, un moyen (112,116) pour éviter la sortie de ladite bascule d'être modifiée tandis que ledit circuit de division par m est réinitialisé en réponse audit premier signal de commande FCS.

2. Dispositif selon la revendication 1 dans lequel ledit moyen de commande produit, de plus, un second signal de commande SCS, initié par une transition dudit signal d'oscillateur FFOS précédant ladite transition prédéterminée et terminé par une transition dudit signal d'oscillateur FFOS suivant ladite transition prédéterminée, de sorte que les fronts avant des impulsions définissant ledit premier signal de commande FCS se produisent entre les fronts respectifs avant et arrière des impulsions associées définissant ledit second signal de commande SCS ; dans lequel ladite bascule comporte une borne d'entrée de signal d'horloge couplée pour recevoir la sortie dudit circuit de division par m et ladite bascule est conditionnée par ledit second signal de commande SCS pour ne pas modifier les états tandis que ledit circuit de division par m est réinitialisé en réponse audit premier signal de commande FCS.

3. Dispositif selon la revendication 2 incluant, de plus:

   une bascule supplémentaire (62) ayant une borne de réinitialisation et ayant une bone d'entrée de signal d'horloge couplée pour recevoir la sortie dudit circuit de division par m : ladite bascule supplémentaire étant disposée pour modifier les états de sortie à chaque fois qu'une transition prédéterminée se produit à sa borne d'entrée de signal d'horloge ;

   une porte OU (64) ayant ses bornes d'entrée respectives couplées pour recevoir l'un desdits premier et second signaux de commande FCS, SCS et le signal de sortie MCS de ladite bascule citée en premier et ayant sa borne de sortie couplée à la borne de réinitialisation de ladite bascule supplémentaire ; et

   une porte ET (66) ayant ses bornes d'entrée respectives couplées pour recevoir la sortie de ladite bascule supplémentaire et ladite sortie dudit circuit de division par m et ayant sa borne de sortie

couplée à la borne d'entrée de signal d'horloge de ladite bascule citée en premier.

4. Dispositif selon la revendication 3 dans lequel ledit moyen diviseur comprend une pluralité d'étages diviseurs (42, 44...48,50) ,ledit dispositif incluant, de plus, un moyen (150) pour verrouiller le présent état desdits étages diviseurs avant que ledit moyen diviseur ne soit réinitialisé en réponse audit premier signal de commande FCS ; ledit moyen de verrouillage comprend une pluralité de bascules (152, 154...158,160) ayant des bornes respectives d'entrée de données couplées pour recevoir les bits respectifs indicateurs de l'état présent desdits étages diviseurs et leurs bornes d'entrée de signal d'horloge couplées pour recevoir ledit second signal de commande de sorte que l'état présent dudit diviseur est verrouillé par lesdites bascules lors de l'apparition de chaque impulsion du second signal de commande SCSP.