What is claimed is:

1. A group III nitride semiconductor device, comprising:

a substrate (1);

a nitride semiconductor layer (2) located on the substrate (1); and

a passivation layer (3) located on the nitride semiconductor layer (2), a portion of the passivation layer (3) in a gate region being etched to expose the nitride semiconductor layer (2) so as to form a gate groove,

which is characterized in that the group III nitride semiconductor device further comprises:

a composite dielectric layer located on the passivation layer (3) and the gate groove, the composite dielectric layer comprising a nitride dielectric layer (41), an oxynitride dielectric layer (42) and an oxide dielectric layer (43) which are formed sequentially in the direction away from the substrate (1);

a source electrode (51) and a drain electrode (52) respectively located in a source region and a drain region on the nitride semiconductor layer (2), and a gate electrode (53) located in a gate region between the source region and the drain region on the composite dielectric layer.

2. The group III nitride semiconductor device according to claim 1, characterized in that the nitride dielectric layer (41) comprises an aluminum nitride dielectric layer in a crystalline state or in an amorphous state.

3. The group III nitride semiconductor device according to claim 2, characterized in that the aluminum nitride dielectric layer has a thickness of less than 4 nm, and preferably less than 2 nm.

4. The group III nitride semiconductor device according to claim 1, characterized in that the oxide dielectric layer (43) comprises one of an aluminum oxide dielectric layer, a silica dielectric layer, a hafnium oxide dielectric layer and any combination thereof.

5. The group III nitride semiconductor device according to claim 1, characterized in that the oxynitride dielectric layer (42) comprises an aluminum oxynitride dielectric layer.

6. The group III nitride semiconductor device according to claim 1, characterized in that in the composite dielectric layer, the nitride dielectric layer (41), the oxynitride dielectric layer (42) and the oxide dielectric layer (43) which are formed sequentially in the direction away from the substrate (1) are stacked periodically and alternately.

7. The group III nitride semiconductor device according to claim 1, characterized in that the nitride semiconductor layer (2) comprises a nitride nucleation layer (21), a nitride buffer layer (22), a nitride channel layer (23) and a nitride barrier layer (24) disposed sequentially in a direction away from the substrate (1).

8. The group III nitride semiconductor device according to claim 7, characterized in that a nitride capping layer (25) is further included between the nitride barrier layer (24) and the passivation layer (3).

9. The group III nitride semiconductor device according to claim 8, characterized in that the nitride capping layer (25) comprises a gallium nitride layer.

10. The group III nitride semiconductor device according to claim 1, characterized in that the nitride barrier layer (24) is etched to form the gate groove inside the nitride barrier layer (24).

11. The group III nitride semiconductor device according to claim 1, characterized in that a nitride insertion layer (26) is further included between the nitride barrier layer (24) and the nitride channel layer (23).

12. The group III nitride semiconductor device according to claim 1, characterized in that the nitride semiconductor layer (2) comprises one of a gallium nitride layer, an indium gallium nitride layer, an aluminum gallium nitride layer, an aluminum gallium indium nitride layer and any combination thereof.

13. A method of manufacturing a group III nitride semiconductor device, comprising:

preparing a substrate (1);

forming a nitride semiconductor layer (2) on the substrate (1); and

forming a passivation layer (3) on the nitride semiconductor layer (2), a portion of the passivation layer (3) in a gate region being etched to expose the nitride semiconductor layer (2) so as to form a gate groove,

which is characterized in that the method further comprises:

forming a composite dielectric layer on the passivation layer (3) and the gate groove, the composite dielectric layer comprising a nitride dielectric layer (41), an oxynitride dielectric layer (42) and an oxide dielectric layer (43) which are formed sequentially in the direction away from the substrate (1);

forming a source electrode (51) and a drain electrode (52) respectively in a source region and a drain region on the nitride semiconductor layer (2), and forming a gate

electrode (53) in a gate region between the source region and the drain region on the composite dielectric layer.

14. The method of manufacturing the group III nitride semiconductor device according to claim 13, characterized in that forming the oxide dielectric layer (43) comprises atomic layer deposition.

15. The method of manufacturing the group III nitride semiconductor device according to claim 13, characterized in that forming the oxynitride dielectric layer (42) comprises:

depositing a nitride dielectric layer;

performing oxidation processing for a surface of the nitride dielectric layer so as to generate the oxynitride dielectric layer (42).