

Circuit arrangement and optical read/write device including the circuit arrangement.

The invention relates to a circuit arrangement having a first and a second supply terminal for connection to a power supply, an input terminal for receiving an input signal, and an output terminal for supplying an output signal, which circuit arrangement further has level-shifting means for effecting a shift in d.c. level of the output signal with respect to the input signal.

The invention further relates to a device for reading and/or writing information in an optical information carrier, including such a circuit arrangement.

A circuit arrangement of the type defined in the opening paragraph enables a signal to be transmitted between two circuits operated with mutually different supply voltages. Such a circuit arrangement is known from US 4,794,283. The known circuit arrangement has an amplifier stage with a first and a second controllable semiconductor element, which semiconductor elements each have a main current path and a control electrode, the main current paths being arranged in series with one another between the supply terminals. The circuit arrangement has a first and a second inverter, the first inverter having an input coupled to a node between the two main current paths and the second inverter having an input coupled to an output of the first inverter. An output of the second inverter forms the output terminal for supplying the level-shifted output signal. Each of the control electrodes of the controllable semiconductor elements is connected to the input terminal via a respective capacitive impedance. Moreover, each of the control electrodes is coupled to the output of the first inverter via its own feedback circuit. The known circuit arrangement can assume a first or a second state, a change-over from one state to the other state being possible in response to a transition in the voltage of the input signal. The known circuit arrangement has the drawback that no change of state occurs if the transition in the input signal is too slow. In this situation the output signal of the circuit arrangement will therefore not be reliable.

It is an object of the invention to provide a circuit arrangement of the type defined in the opening paragraph which also supplies a reliable output signal in the case of slow transitions in the input signal. To achieve said object, the invention is characterized in that the level-shifting means include a current source and resistive means, the output terminal

being connected to an output of the current source and the output terminal being connected to the input terminal via the resistive means. When the input terminal is connected to a low-impedance signal source and the output is connected to a high-impedance input of a receiving circuit a current, determined by the current source, flows through the resistive means and produces a voltage drop across the resistive means. This voltage drop results in a shift in d.c. level between the signal on the input terminal and the signal on the output terminal. Low-frequency components of the signal on the input terminal can also reach the output terminal unimpeded, as a result of which the signal on the output terminal also tracks slow transitions of the input signal in a reliable manner. The circuit arrangement in accordance with invention is suitable for shifting the levels both of digital signals and of analog signals.

In a favorable embodiment the circuit arrangement has a reference voltage source for supplying a reference voltage and has a further input terminal for receiving a bias voltage, the circuit arrangement further including setting means for setting the current generated by the current source to a value which is a function of the difference between the reference voltage and the bias voltage. Since the current generated by the current source is a function of the voltage difference between the reference voltage and the bias voltage the desired d.c. level in the present embodiment can be set by means of the bias voltage on the reference terminal.

An advantageous embodiment of the circuit arrangement in accordance with the invention is characterized in that the bias voltage and the input signal are supplied by circuits which are powered with mutually the same supply voltage. Disturbances in the input signal as a result of variations in the supply voltages give rise to corresponding disturbances in the bias voltage. This results in the disturbances being cancelled out in the afore-mentioned favorable embodiment of the circuit arrangement.

A practical variant of this embodiment is characterized in that the reference voltage source is connected to the further input terminal via further resistive means, and the current source comprises an output branch of a first current mirror having an input branch which is also connected to the further input terminal via the further resistive means, the output branch being connected to the output terminal. When the further input terminal is connected to a bias voltage source a current which depends on the voltage supplied by the bias voltage source will flow via the further resistive means and the input branch of the current mirror. In the output branch the current mirror generates a current which is proportional to the current through the input branch, which results in a voltage drop across the resistive means which is proportional to the voltage drop across the further resistive means. Preferably, the current

mirror, the resistive means and the further resistive means are dimensioned in such a manner relative to one another that the voltage drop across the resistive means is equal to the voltage drop across the further resistive means. The resistive means and the further resistive means for example have mutually the same resistive values and the current mirror is a 1:1 current mirror.

- 5 In a practical embodiment of the circuit arrangement the reference voltage source comprises a voltage divider having first and second resistive means the reference output being formed by a first tap of the voltage divider, which tap is connected to the first supply terminal via the first resistive means and to the second supply terminal via the second resistive means, the setting means comprising a first controllable semiconductor element having a main current path and a control electrode, the reference output being connected to the further resistive means via the control electrode of the first controllable semiconductor element.

- In this embodiment the voltage divider operates as the reference voltage source. The voltage divider supplies a substantially constant voltage to the control electrode of the first controllable semiconductor element. As a result of this, the voltage on the main electrode of the controllable semiconductor element to which the further resistive means are connected is also substantially constant. The current through the further resistive means is mainly supplied by the input branch of the first current mirror via the main current path of the first controllable semiconductor element.

- An attractive embodiment of the circuit arrangement in accordance with the invention is characterized in that the current source further includes an output branch of a second current mirror, one of said first and second current mirrors being a current-draining current mirror and the other one of said current mirrors being a current-supplying current mirror, an input branch of the second current mirror being also connected to the further input terminal via the further resistive means and the output branch of the second current mirror being connected to the output terminal. This embodiment has the advantage that the d.c. level of the signal on the output terminal can be set to a higher as well as to a lower value with respect to the signal on the input terminal.

- In another attractive embodiment the setting means comprise a first and a second controllable semiconductor element and the reference voltage source comprises a voltage divider having first and second resistive means and a third and a fourth controllable semiconductor element the current source further comprising an output branch of a second current mirror, one of said first and second current mirrors being a current-draining current mirror and the other one of said current mirrors being a current-supplying current mirror, said semiconductor elements each having a main current path and a control electrode the control electrode of the first

semiconductor element and the control electrode of the third semiconductor element being connected to a first tap of the voltage divider, the control electrode of the second semiconductor element and the control electrode of the fourth semiconductor element being connected to a second tap of the voltage divider, the first tap of the voltage divider being
5 connected to the first supply terminal via the first resistive means and to the second supply terminal via the second resistive means, which setting means have a node connected to the input branch of the first current mirror via the main current path of the first controllable semiconductor element and to the input branch of the second current mirror via the main current path of the second semiconductor element, the further input terminal being connected
10 to the node via the further resistive means, and the first tap and the second tap of the voltage divider being connected to one another via the main current path of the third semiconductor element and the main current path of the fourth semiconductor element. In the present embodiment a current whose value is mainly determined by the resistive values of the resistive means flows via the voltage divider formed by the first resistive means, the third
15 semiconductor element, the fourth semiconductor element and the second resistive means. The voltage on the node settles at a value which is approximately equal to the average of the voltages on the taps of the voltage divider.

Preferably, the resistive means and the further resistive means are each shunted by capacitive means. By shunting the resistive means it is achieved that high-frequency
20 variations at the input terminal are transferred to the output terminal in a better manner. Shunting of the further resistive means provides compensation for high-frequency variations in the input signal which have been caused by supply voltage variations.

The circuit arrangement in accordance with the invention is very suitable for use in a device for reading/and/or writing of information in an optical data carrier.

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These and other aspects of the invention will be elucidated with reference to the drawings. In the drawings:

Figure 1 shows a first embodiment of the circuit arrangement in accordance with the invention,

30 Figure 2 shows a second embodiment of the circuit arrangement in accordance with the invention,

Figure 3 shows a third embodiment of the circuit arrangement in accordance with the invention,

Figure 4 diagrammatically shows a device in accordance with the invention for reading and/or writing information in an optical information carrier,

Figure 5 shows the device of Figure 4 in greater detail,

Figure 6 is a view as indicated by an arrow VI in Figure 5, and

5 Figure 7 shows a part of the device of Figure 4 in greater detail.

Figure 1 shows a circuit arrangement having a first supply terminal 1 and a second supply terminal 2 for receiving a high supply voltage V_{dd} and a lower supply voltage V_{ss} , respectively. The circuit arrangement further has an input terminal 3 for receiving an
10 input signal. The circuit arrangement further has level-shifting means 5, 6 for producing on an output terminal 4 a signal S_o which has been shifted in d.c. level with respect to the input signal. The level-shifting means comprise a current source 5 and resistive means 6. The output terminal 4 is connected to an output of the current source 5, and resistive means formed by a resistive impedance 6 connect the output terminal 4 to the input terminal 3.

15 The circuit arrangement shown in Figure 1 operates as follows. When a voltage signal source which supplies a voltage signal S_i is connected to the input terminal 3 a current I flows from the current source 5 to the voltage signal source via the resistive impedance 6. As a result of this, a voltage drop is produced across the resistive impedance 6. This results in a signal S_o on the signal terminal, which signal has been shifted in d.c. level with respect to the
20 input signal S_i . Any desired shift in d.c. level can be achieved by an appropriate choice of the polarity and the magnitude of the current I and the magnitude of the resistive impedance 6.

The embodiment of the circuit arrangement in accordance with the invention shown in Figure 1 has a further input terminal 7 for receiving a bias voltage S_{is} . The further input terminal 7 is connected to an output 9 of a reference voltage source 10 via further
25 resistive means formed by a further resistive impedance 8. The circuit arrangement further includes setting means 11 for setting the current I generated by the current source 5 to a value which is a function of the current I' through the further resistive means 8. When the further input terminal 7 is connected to a bias voltage source a current I' is produced through the further resistive means 8, which current is proportional to the voltage difference between the
30 voltage on the output 9 of the reference voltage source and the voltage S_{is} supplied by the bias voltage source and appearing on the further input terminal 7. With the aid of the setting means 11 it is achieved that the current I generated by the current source 5 is set to a value which is a function of the current I' through the further resistive means 8. Thus, the shift in d.c. level in

the circuit arrangement in accordance with the invention shown in Figure 1 can be set to the desired value by means of an external voltage source.

In Figure 2 parts corresponding to those in Figure 1 bear the same reference numerals. Figure 2 shows a practical variant of the embodiment shown in Figure 1. In this variant the reference voltage source 10 comprises a voltage divider 12, 13. The semiconductor element 14 has a control electrode 143 and a main current path between main electrodes 141, 142. The control electrode 143 is connected to a first tap 9 of the voltage divider 12, 13, which tap forms a reference output. The voltage divider 12, 13 has first resistive means 12 and second resistive means 13, the first tap 9 of the voltage divider being connected to the first supply terminal 1 via the first resistive means 12 and to the second supply terminal 2 via the second resistive means 13. The current source 5 is formed by a first current mirror having an input branch 16 and an output branch 17. The reference output 9 is connected to the input branch 16 of the first current mirror via the control electrode of the first controllable semiconductor element 14. The first controllable semiconductor element 14 and the input branch 17 of the first current mirror together form setting means. The output branch 17 of the current mirror is connected to the output terminal 4. The current mirror may have more than one output branch. In the present embodiment the current mirror has a further output branch 18 connected to a further output terminal 21. The further output terminal 21 is connected to a further input terminal 20 via a resistive impedance 19. The input branch 16 is formed by a main current path of a diode-connected controllable semiconductor element 21. The output branch 17 and the further output branch 18 are formed by respective main current paths of controllable semiconductor elements 22 and 22'. The control electrodes of the semiconductor elements 21, 22 and 22' are coupled to one another. Each of the semiconductor elements have a main element coupled to the first supply terminal 1.

In the embodiment shown in Figure 2 the voltage divider 12, 13 operates as the reference voltage source. The voltage divider 12, 13 supplies a substantially constant voltage to the control electrode 143 of the first controllable semiconductor element 14. There is a substantially constant voltage difference between the control electrode 143 and the main electrode 142, as a result of which the voltage on the main electrode 142 is also substantially constant. Via the input branch 16 of the first current mirror the main current path of the first controllable semiconductor element 14 supplies a current I' which is approximately proportional to the difference between the reference voltage on the reference output 9 and the bias voltage S_{is} on the input terminal 7. This current I' is replicated by the current mirror, as a result of which a voltage drop is produced across the resistive impedance 6, which voltage

drop is proportional to the voltage drop across the further resistive impedance 8. Preferably, the current mirror, the resistive impedance 6 and the further resistive impedance 8 are so proportioned with respect to one another that the voltage drop across the resistive impedance 6 is equal to that across the further resistive impedance 8. For example, the resistive impedance 6 and the further resistive impedance 8 have equal resistive values and the current mirror is a 1:1 current mirror.

In Figure 3 parts bearing the same reference numerals correspond to those in Figure 2. Likewise, the parts 9A, 14A, 16A, 17A, 21A and 22A respectively correspond to the parts 9, 14, 16, 17, 21 and 22 in Figure 2. In the embodiment of the circuit arrangement in accordance with the invention shown in Figure 3 the current source comprises an output branch 17A of the current-supplying first current mirror and an output branch 17B of the current-draining second current mirror. The output of the current source is formed by a node 27 between said output branches 17A, 17B.

The circuit arrangement further has a second controllable semiconductor element 14B, a third controllable semiconductor element 24A and a fourth 24B controllable semiconductor element each having a main electrode and a main current path. The input branch 16B of the second current mirror is connected to a node 15 via the main current path of the second controllable semiconductor element 14B. The first resistive impedance 12 and the second resistive impedance 13 of the voltage divider are connected to one another via the successive main current paths of the third controllable semiconductor element 24A and the fourth controllable semiconductor element 24B. The third controllable semiconductor element 24A has its control electrode 24A3 connected to the control electrode 14A3 of the first controllable semiconductor element 14A. The control electrode 24B3 of the fourth controllable semiconductor element 24B and the control electrode 14B3 of the second controllable semiconductor element 14B are connected to one another and to a second tap 9B of the voltage divider. The first tap 9A is connected to the second tap 9B via the main current path of the third controllable semiconductor element 24A and the main current path of the fourth controllable semiconductor element 24B. In the present embodiment the resistive impedances 8 and 6 are shunted by the capacitive impedances 25 and 26, respectively.

In the situation shown in Figure 3 the circuit arrangement is connected to a further circuit 30 having supply terminals 31, 32 connected to supply voltages V_{dd}' , V_{ss}' which differ from the supply voltages V_{dd} , V_{ss} to which the circuit arrangement is connected. The further circuit 30 has a signal source 36 which supplies the signal S_i to the input terminal 3 of the circuit. The signal S_i has a d.c. level which is approximately equal to $(V_{dd}' + V_{ss}')/2$.

The further circuit 30 further has a bias voltage source formed by the resistive impedances 33 and 34 and an operational amplifier 35. In the case of equal resistive values of the resistive impedances 33, 34 the bias voltage source supplies a bias voltage S_{is} equal to $(V_{dd}' + V_{ss}')/2$.

The circuit arrangement shown in Figure 3 operates as follows. When the supply terminals 1, 2 are connected to the supply voltages V_{dd} and V_{ss} a current I_b will flow via the resistive impedance 12, the third semiconductor element 24a, the fourth semiconductor element 24B and the resistive impedance 13. The value of the current I_b is mainly determined by the resistive values of the resistive impedances 12 and 13. It is assumed that the resistive impedances 12 and 13 have equal resistive values R . However, this is not necessary.

If the further input terminal 7 has not been connected the circuit arrangement assumes a neutral state, in which substantially the same voltage drops appear between the electrodes 14A1 and 14A3, between the electrodes 14B1 and 14B3, between the electrodes 24A1 and 24A3, and between the electrodes 24B1 and 24B3. The node 15 is then at a voltage V_{ref} which is approximately $(V_{dd} + V_{ss})/2$. Through the main current paths of the first semiconductor element 14A and the second semiconductor element 14B a quiescent current flows which has approximately the same magnitude and the same direction as the current I_b via the third semiconductor element 24A and the fourth semiconductor element 24B. In this situation the input branch 16A and the output branch 17A of the first current mirror also supply a current I_b . The input branch 16B and the output branch 17B of the second current mirror each drain a current I_b . In this situation the output branch 17B of the second current mirror drains a current equal to the current supplied by the output branch 17A of the first current mirror. The current source formed by the output branches 17A, 17B of the current mirrors then generates no current and, consequently, does not produce a voltage drop across the resistive impedance 6.

When the further input terminal 7 is connected to a bias voltage source having a bias voltage S_{is} lower than the reference voltage V_{ref} a current I' will flow from the node 15 to the further input terminal 7 via the further resistive impedance 8. The first semiconductor element 14A then operates in such a manner that the voltage drop across the electrodes 14A1 and 14A3 has slightly increased and a current which is approximately equal to $I_b + I'/2$ flows through its main current path. This current is supplied by the input branch 16A of the first current mirror. Thus, the first current mirror also supplies a current $I_b + I'/2$. The second semiconductor element 14B then operates in such a manner that the voltage drop across the electrodes 14B1 and 14AB has slightly decreased and a current which is approximately equal to $I_b - I'/2$ flows through its main current path. This current is drained by the input branch 16B

of the second current mirror. Thus, the output branch of the second current mirror also drains a current $I_b - I/2$. The current source formed by the output branches 17A, 17B of the current mirrors then supplies a current I' and consequently produces a voltage drop across the resistive impedance 6, which voltage drop corresponds to that across the further resistive impedance 8.

5 In the case that the bias voltage source supplies a bias voltage S_{is} higher than the reference voltage V_{ref} a current I' will flow from the further input terminal 7 to the node 15. The first semiconductor element 14A is now given a setting in which the voltage across the electrodes 14A1 and 14A3 has increased slightly with respect to the neutral state and in which a current $I_b - I/2$ flows via the main current path of the first semiconductor element 14A. The
10 second semiconductor element 14B is now given a setting in which the voltage across the electrodes 14B1 and 14B3 has slightly increased with respect to the neutral state and in which a current $I_b + I/2$ flows via its main current path. In this situation the current source formed by the output branches 17A, 17B of the current mirrors drains a current I' and thereby produces another voltage drop across the resistive impedance 6, which voltage drop corresponds to that
15 across the further resistive impedance 8.

Thus, the desired shift in d.c. level of the output signal S_o with respect to the input signal can be controlled by means of the bias voltage S_{is} . In the combination of the circuit arrangement 0 and the further circuit 30, shown in Figure 3, the shift in d.c. level of the output signal S_o with respect to the input signal S_i is equal to the difference between $(V_{dd} + V_{ss})/2$ and $(V_{dd}' + V_{ss}')/2$. As a result of this, the supply voltages for the circuit arrangement
20 0 and the further circuit 30 can be chosen independently of one another.

The bias voltage S_{is} and the input signal S_i are supplied by circuits 35, 36 which are powered with mutually the same supply voltage V_{dd}' , V_{ss}' . This has the advantage that variations in the input signal S_1 which are attributable to variations in the supply voltage
25 V_{dd}' , V_{ss}' are compensated for by complementary variations in magnitude of the shift in d.c. level.

The embodiment shown in Figure 3 can shift a single signal S_i in d.c. level with the aid of the level-shifting means 22A, 17A, 17B, 22B, 6, 3 and 4. On the other hand, the present circuit arrangement, similarly to the circuit arrangement shown in Figure 2, may have
30 a plurality of level-shifting means. This enables a plurality of signals to be shifted in d.c. level without additional setting means being required.

What types of controllable semiconductor elements are used in the circuit arrangement in accordance with the invention is irrelevant for the essence of the invention.

Suitable semiconductor technologies for realizing the circuit arrangement are, for example, CMOS, bipolar technology or BICMOS.

The level-shifting means in accordance with the invention are particularly suitable for use in a device for reading and/or writing information in an optical information carrier. Such a device is shown in Figure 4.

The information carrier 51 is, for example, of a write-once type, for example an information carrier of the ablative type. The information carrier may also be of a rewritable type, for example an information carrier having an information layer of a material having an amorphous structure which can locally be transformed into a crystalline structure by successively heating and cooling the information layer. Such a material is, for example, an alloy of Te, Se and Sb. Alternatively, the information carrier may, for example, be of the magneto-optical type. These information carriers have an information layer of a magnetizable material. The magnetization is influenced by heating the information layer locally beyond the Curie temperature, for example by means of a laser beam, and at the same time exposing it to a magnetic field.

The device includes a control unit 57 for generating a pulsed transducer control signal S_{Storage} in response to an information signal S_{Info} in a first mode of operation. The information signal is generated from an input signal S_i . An error correction encoding is applied with the aid of the error correction encoding means 58. The information signal S_{Info} is subsequently derived from the resulting signal by channel encoding with the aid of channel encoding means 59. The channel encoding means 59 are, for example, EFM or EFM + channel encoding means.

During information recording the transducer 60 generates physically detectable patterns in the information layer 52 of the information carrier 51 in response to the transducer control signal S_t .

The device has a second mode of operation for reading information from an information carrier 51. The information carrier 51 can be an information carrier provided with information by means of the device described hereinbefore but can alternatively be an information carrier obtained in another way, for example in another device, for example a device in which patterns are formed in the information layer by pressing. In the device shown the transducer 60 is also adapted to generate a read signal S_r in response to physically detectable patterns in the information carrier. The transducer 60 for the generation of the read signal comprises a radiation source 61. The device further has a power supply, in the present case formed by the control unit 57, which powers the radiation source 61 with electric power.

The power supply receives a signal S_p from the transducer, which signal is a measure of the intensity of the radiation emitted by the radiation source. A control mechanism which forms part of the power supply 57 is responsive to this signal S_p to control the power supplied to the radiation source 62 in such a manner that the intensity of the radiation emitted by the radiation source is not influenced by aging and/or warming-up of the radiation source 61. Another control mechanism may be provided in order to adapt the power supplied to the radiation source 61 to the condition of the information carrier 51, in such a way that for example in the case of fingermarks on the information carrier 51 the write signal can yet be recorded in a reliable manner. Such a control mechanism can make use of a signal which is a measure of the intensity of radiation reflected from the information carrier.

In the embodiment shown the device is adapted to read and write information from/to a disc-shaped information carrier 51. For this purpose, the device has a motor 63 for making the information carrier rotate and a control unit 64 for controlling the motor 63. The radial position of the transducer 60 is determined by a servo-system 65. The servo-system 65 and the control unit 64 are controlled by a microprocessor 66. The motor 63, the control unit 64, the servo-system 65 and the microprocessor 66 are of conventional types.

In the embodiment shown the transducer 60 is used both when information is written onto the information carrier and when information is read from the information carrier 51. Alternatively, different transducers may be used for writing and for reading information. The transducer 60 is shown in greater detail in Figure 5. In addition to the radiation source 61 the transducer 60 includes an optical system, a first detector 70 and a second detector 71. The optical system includes a first beam splitter 72, a lens 73, a second beam splitter 74, a focusing objective 75 and an astigmatic element 76. The second detector 71 has been divided into subdetectors, at least subdetectors being arranged at opposite sides of a line 77 (see Figure 6) which extends in a direction of a track to be written onto an information carrier 51. During information recording the radiation source 61 generates a radiation beam in response to the control signal S_t . The first beam splitter 72 projects a fraction of the radiation in the radiation beam onto the first detector 70. The output signal S_p supplied by the first detector 70 is applied to the power supply unit 57 in order to adapt the power supplied to the radiation source 61 to the response of the radiation source 61 to the applied power. The radiation beam is further imaged onto the information layer 52 of the information carrier 51 by the lens 73, via the beam splitter 74 and by means of the focusing objective 75 and produces a physically detectable, in the present case an optically detectable, effect in said layer. In the second mode of operation of the device the radiation source 61 also generates a radiation beam. In the same

way as in the first mode of operation the radiation beam is imaged onto the information layer 52. Depending on the optically detectable effect the information layer 52 reflects more radiation or less radiation. The reflected radiation is imaged onto the detector 71 via the focusing objective 75, the beam splitter 74 and the astigmatic element 76. In response to the radiation incident on it the detector 71 generates a signal, in the present case a quadruple signal. A preprocessor derives a signal FE, a signal FP and the read signal SIs from the quadruple signal. The servo-system 65 uses the signal FE for focus control of the radiation beam on the information carrier 51. The servo-system uses the signal PP for the radial positioning of the transducer 60.

With the aid of error correction decoding means 80 and channel decoding means 81 an output signal Sout is derived from the read signal.

The power supply unit 57 for the radiation source 61 is shown in greater detail in Figure 7. The power supply unit 57 shown has a first circuit 110 which is energized with a first and a second supply voltage V_{ss}' and V_{dd}' and a second circuit 120 which is energized with a third and a fourth supply voltage V_{ss} and V_{dd} , V_{ss}' differing from V_{ss} and V_{dd}' differing from V_{dd} . The voltages V_{dd} , V_{dd}' and V_{ss}' are supplied by a power supply source (not shown), the voltage V_{ss}' being obtained via ground. The voltage V_{ss} is derived from the voltages V_{dd} and V_{ss}' by means of a voltage regulator 121 and a resistive impedance 122. The voltage regulator 121 is, for example, a breakdown element such as a zener diode. The second circuit 120 further includes a circuit 124 for generating the signal S_{info}' , which is shifted in d.c. level with respect to the signal S_{info} and the signal L_p' which is shifted in d.c. level with respect to the signal L_p . The signal L_p is a control signal for controlling the average power to be consumed by the radiation source 61. The circuit 124 corresponds to the circuit arrangement shown in Figure 2. Alternatively, a circuit arrangement in an embodiment as shown in Figure 3 may be used. A pulse-generating circuit derives a pulsating signal S_p from the d.c. level-shifted signal S_{info}' . Said signal S_p is applied to a control circuit 126 for controlling a controllable semiconductor element 127 for the power supply to the radiation source 61. The radiation source 61 is included in the main current path of the semiconductor element 127. The control circuit 126 also receives the d.c. level-shifted signal L_p' . The section comprising the semiconductor element 127 and the radiation source 61 is shunted by a capacitive impedance 140. As a result of this, the comparatively large high-frequency currents necessary for driving the radiation source 61 flow mainly via the circuit formed by the semiconductor element 127, the radiation source 61 and the capacitive impedance 140.

It is to be noted that the protective scope of the invention is not limited to the embodiments disclosed in the preceding description. The protective scope of the invention is neither limited by the reference symbols used in the Claims. The use of the verb "to comprise" does not exclude the presence of other elements than those given in a Claim. Moreover, the
5 use of the indefinite article "a" before an element does not exclude the presence of a plurality of such elements.

CLAIMS:



1. A circuit arrangement having a first and a second supply terminal (1 and 2, respectively) for connection to a power supply (V_{dd} , V_{ss}), an input terminal (3) for receiving an input signal (S_i), and an output terminal (4) for supplying an output signal (S_o), which circuit arrangement further has level-shifting means (5, 6) for effecting a shift in d.c. level of the output signal (S_o) with respect to the input signal (S_i),

characterized in that

the level-shifting means include a current source (5) and resistive means (6), the output terminal (4) being connected to an output of the current source (5) and the output terminal (4) being connected to the input terminal (3) via the resistive means (6).

2. A circuit arrangement as claimed in Claim 1, characterized in that the circuit arrangement has a reference voltage source (10) for supplying a reference voltage and has a further input terminal (7) for receiving a bias voltage (S_{is}), the circuit arrangement further including setting means (11) for setting the current (I) generated by the current source (5) to a value which is a function of the difference between the reference voltage and the bias voltage.

3. A circuit arrangement as claimed in Claim 2, characterized in that the bias voltage (S_{is}) and the input signal (S_i) are supplied by circuits (35, 36) which are powered with mutually the same supply voltage (V_{dd}' , V_{ss}').

4. A circuit arrangement as claimed in Claim 2 or 3, characterized in that the reference voltage source (12, 13) is connected to the further input terminal (7) via further resistive means (8), and the current source (5) comprises an output branch (17) of a first current mirror having an input branch (16) which is also connected to the further input terminal (7) via the further resistive means (8), the output branch (17) being connected to the output terminal (4).

5. A circuit arrangement as claimed in Claim 4, characterized in that the reference voltage source (10) comprises a voltage divider (12, 13) having first and second resistive



means (12, 13), the reference output (9) being formed by a first tap of the voltage divider, which tap is connected to the first supply terminal (1) via the first resistive means (12) and to the second supply terminal (2) via the second resistive means (13), the setting means (11) comprising a first controllable semiconductor element (14) having a main current path and a control electrode (143), the reference output (9) being connected to the further resistive means (8) via the control electrode (143) of the first controllable semiconductor element (14).

6. A circuit arrangement as claimed in Claim 4, characterized in that the current source further includes an output branch (17B) of a second current mirror, one of said first and second current mirrors being a current-draining current mirror and the other one of said current mirrors being a current-supplying current mirror, an input branch (16B) of the second current mirror being also connected to the further input terminal (7) via the further resistive means (8) and the output branch (17B) of the second current mirror being connected to the output terminal (4).

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7. A circuit arrangement as claimed in Claim 4, characterized in that the setting means (11) comprise a first and a second controllable semiconductor element (14A and 14B, respectively), and the reference voltage source (10) comprises a voltage divider (12, 13) having first and second resistive means (12 and 13, respectively) and a third and a fourth controllable semiconductor element (24A, 24B), the current source further comprising an output branch (17B) of a second current mirror, one of said first and second current mirrors being a current-draining current mirror and the other one of said current mirrors being a current-supplying current mirror, said semiconductor elements each having a main current path and a control electrode (14A3, 14B3, 24A3 and 24B3, respectively), the control electrode (14A3) of the first semiconductor element (14A) and the control electrode (24A3) of the third semiconductor element (24A) being connected to a first tap (9A) of the voltage divider, the control electrode (14B3) of the second semiconductor element (14B) and the control electrode (24B3) of the fourth semiconductor element (24B) being connected to a second tap (9B) of the voltage divider, the first tap (9A) of the voltage divider being connected to the first supply terminal (1) via the first resistive means (12) and to the second supply terminal (2) via the second resistive means (13), which setting means have a node (15) connected to the input branch (16) of the first current mirror via the main current path of the first controllable semiconductor element (14) and to the input branch (16B) of the second current mirror via the main current path of the second semiconductor element (14B), the further input terminal (7)

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being connected to the node (15) via the further resistive means (8), and the first tap (9A) and the second tap (9B) of the voltage divider (12, 13) being connected to one another via the main current path of the third semiconductor element (24A) and the main current path of the fourth semiconductor element (24B).

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8. A circuit arrangement as claimed in any one of the Claims 2 through 7, characterized in that the resistive impedance (6) and the further resistive impedance (8) are each shunted by a capacitive impedance (26 and 25, respectively).

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9. A device for reading and/or writing information in an optical information carrier (51), which device has a first circuit (110) connected to a first pair of supply voltages (V_{dd}' , V_{ss}') and has a second circuit (124) connected to a second pair of supply voltages (V_{dd} , V_{ss}), which second circuit has been equipped with a circuit arrangement as claimed in any one of the Claims 1 through 8, via which circuit arrangement the first circuit transfers a signal (L_p)

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to the second circuit, which device further includes error correction encoding means (58) and/or channel encoding means (59) for deriving an information signal (S_{info}) from an input signal (S_{in}) by means of error correction encoding and/or channel encoding, and/or includes error correction decoding means (80) and/or channel decoding means (81) for deriving an output signal (S_{out}) from a read signal (S_{ls}) by means of error correction decoding and/or

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channel decoding.