

METHOD OF FABRICATING A SILICON TUNNELING FIELD EFFECT TRANSISTOR (TFET) WITH HIGH DRIVE CURRENT

ABSTRACT

A method (and semiconductor device) of fabricating a TFET device provides a source region having at least a portion thereof positioned underneath a gate dielectric. In one embodiment, the TFET includes an N⁺ drain region and a P⁺ source region in a silicon substrate, where the N⁺ drain region is silicon and the P⁺ source region is silicon germanium (SiGe). The source region includes a first region of a first type (e.g., P⁺ SiGe) and a second region of a second type (undoped SiGe), where at least a portion of the source region is positioned below the gate dielectric. This structure decreases the tunneling barrier width and increases drive current (I_d).

Fig. 4