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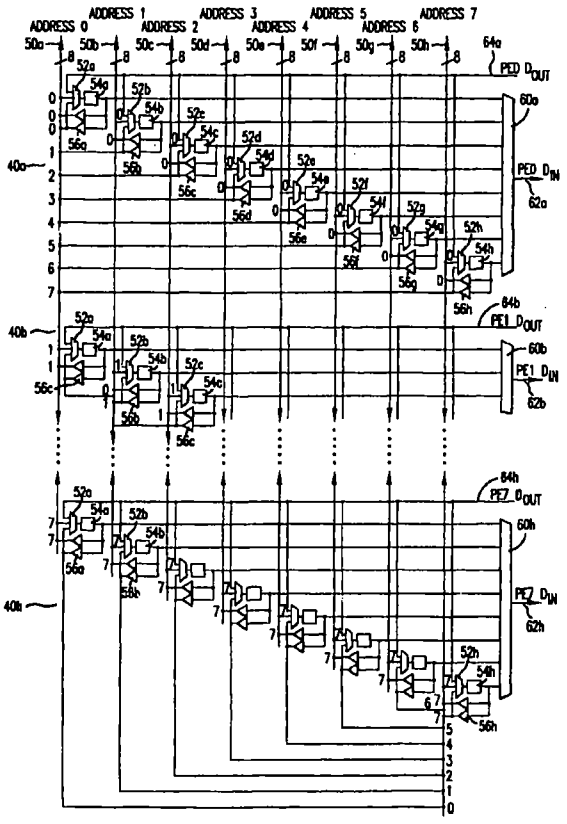
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(54) Title: METHOD AND APPARATUS FOR CONNECTING A MASSIVELY PARALLEL PROCESSOR ARRAY TO A MEMORY ARRAY IN A BIT SERIAL MANNER



(57) Abstract: A method and apparatus for connecting the processor array of an MPP array to a memory such that data conversion by software is not necessary, and the data can be directly stored in either a normal mode or vertical mode in the memory is disclosed. A connection circuit is provided in which multiple PEs share their connections to multiple data bits in the memory array. Each PE is associated with a plurality of memory buffer registers, which stores data read from (or to be written to) one or two memory data bits. In horizontal (normal) mode connection the memory bits are selected so that all the bits of a given byte are stored in the same PE, i.e., each set of buffer registers associated with a respective PE contains one byte as seen by an external device. In vertical (bit serial) mode, each set of buffer registers contains the successive bits at successive locations in the memory corresponding to that PEs position in the memory word. The selection is achieved utilizing a multiplexer on the input to the register and a pair of tri-state drivers which drive each data line.

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