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A METHOD TO FORM ELEVATED SOURCE/DRAIN USING POLY SPACER

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BACKGROUND OF THE INVENTION

(1) Field of the Invention

The invention relates to the fabrication of integrated circuit devices, and more particularly, to a method of forming an elevated source/drain MOSFET structure in the fabrication of integrated circuits.

(2) Description of the Prior Art

As devices are scaled down, short channel effects become severe. That is, as the dimensions of the gate are reduced, the threshold voltage of the MOSFET becomes less predictable. Short channel effects cause source/drain leakage and voltage roll-off. To prevent short-channel effects, shallow source/drain junctions must be used. However, shallow junctions cause problems when forming salicide, such as junction leakage. An elevated source/drain structure can reduce short channel effects without these problems.

A number of workers in the art have proposed elevated source/drain structures. U.S. Patent 5,386,133 to Hiroki, 5,631,482 to Hong, and 5,684,319 to

Hebert disclose methods of forming polysilicon spacers as source/drain contacts. U.S. Patent 4,488,162 to Jambotkar shows a raised source/drain process.

SUMMARY OF THE INVENTION

A principal object of the present invention is to provide an effective and very manufacturable method of forming a MOSFET having an elevated source/drain structures.

A further object of the invention is to provide a method of forming a sub-quarter micron MOSFET having an elevated source/drain structure wherein short channel effects are reduced.

Yet another object is to provide a method of forming a sub-quarter micron MOSFET having an elevated source/drain structure wherein source/drains are extended by outdiffusion from the elevated source/drains.

In accordance with the objects of this invention a method for forming a sub-quarter micron MOSFET having an elevated source/drain structure is achieved. A gate electrode is formed over a gate dielectric on a semiconductor substrate. Ions are implanted into the

semiconductor substrate to form lightly doped regions using the gate electrode as a mask. Thereafter, dielectric spacers are formed on sidewalls of the gate electrode. A polysilicon layer is deposited overlying the semiconductor substrate, gate electrode, and dielectric spacers wherein the polysilicon layer is heavily doped. The polysilicon layer is etched back to leave polysilicon spacers on the dielectric spacers. The polysilicon spacers form elevated source/drain regions. Dopant is diffused from the polysilicon spacers into the semiconductor substrate to form source and drain extension regions underlying the elevated source/drain regions. The polysilicon spacer on an end of the gate electrode is removed to separate the elevated source/drain regions into an elevated source region and an elevated drain region thereby completing formation of a MOSFET having an elevated source/drain structure in the fabrication of an integrated circuit device.

BRIEF DESCRIPTION OF THE DRAWINGS

In the accompanying drawings forming a material part of this description, there is shown:

Figs. 1 through 7A schematically illustrate in cross-sectional representation a preferred embodiment of the

present invention.

Fig. 7B schematically illustrates in cross-sectional representation an optional process in a preferred embodiment of the present invention.

Figs. 8 and 9 schematically illustrate in top view a preferred embodiment of the present invention.

Fig. 10 illustrates a completed integrated circuit device fabricated according to the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring now more particularly to Fig. 1, there is shown an illustration of a portion of a partially completed metal oxide field effect transistor (MOSFET). The semiconductor substrate 10 is preferably composed of silicon having a (100) crystallographic orientation and has been doped to be a p-type substrate. It will be understood by those skilled in the art that while Figs. 1 through 10 illustrate an N channel MOSFET integrated circuit device, a P channel FET integrated circuit device could be formed simply by substituting opposite polarities to those given for the N channel embodiment. Also, in a similar way, a CMOSFET could

be formed by making both N channel and P channel devices upon the same substrate.

In an effort to simplify the description and the drawings the dielectric isolation between devices has been only partially shown and will not be described in detail, because they are conventional. For example, shallow trench isolation region 11 can be formed in the semiconductor substrate, as shown.

A gate dielectric layer 14 is formed on the surface of the semiconductor substrate, for example, using thermal oxidation to form a silicon dioxide layer having a thickness of between about 10 and 100 Angstroms. Next, a polysilicon layer 16 is deposited over the gate dielectric layer to a thickness of between about 1000 and 4000 Angstroms by low pressure chemical vapor deposition (LPCVD), for example.

Referring now to Fig. 2, the polysilicon layer and gate dielectric layer are patterned to form a gate electrode 16. Ions are implanted into the surface of the substrate, using the gate electrode as a mask, to form lightly doped regions 22. For example, the lightly doped regions 22 may be formed by implanting ions into the

substrate at an energy of 0.1 to 50 KeV and dosage of 10^{13} to 10^{15} atoms/cm^2. For NMOS, phosphorus ions are implanted while for PMOS, boron ions are implanted.

Now, a dielectric layer, such as an oxide layer, 24 is deposited over the substrate and the gate electrode to a thickness of between about 25 and 200 Angstroms, as shown in Fig. 3. The oxide layer could be thermally grown, but deposited oxide is preferred because of better uniformity.

The oxide layer 24 is anisotropically etched back to leave oxide spacers 26 on the sidewalls of the gate 16. The oxide is removed on top of the gate electrode and on top of the lightly doped regions 22, as shown in Fig. 4.

A second polysilicon layer 30 is blanket deposited over the gate electrode and the substrate, as shown in Fig. 5. The polysilicon layer is deposited, for example, by LPCVD to a thickness of between about 500 and 4000 Angstroms. The polysilicon layer is heavily doped with an N+ dopant (or with a P+ dopant for the PMOS case) in the concentration of between about 10^{20} and 10^{22} atoms/cm^3. The polysilicon layer may be doped in-situ to save process steps or may be doped by ion implantation after deposition.

Referring now to Fig. 6, the polysilicon layer 30 is anisotropically etched back to leave polysilicon spacers 32 on the sidewalls of the gate electrode and separated from the gate electrode by the oxide spacers 26. The polysilicon spacers 32 will form the elevated source and drain regions.

After formation of the polysilicon spacers, a thermal cycle is used to drive in the dopant to form source/drain extensions 34 within the substrate underlying the elevated source/drain structures 32, as illustrated in Fig. 7A. For example, the thermal cycle could be a rapid thermal process (RTP) at 800 to 1100 °C for 10 to 50 seconds.

This completes the formation of the MOSFET with elevated source/drain structure. The outdiffused junction is very shallow, thus avoiding short channel effects. At the same time, the elevated polysilicon source/drain 32 does not present problems when forming salicide. The elevated source and drain can be salicided without junction leakage issues. Salicide layer 36 is illustrated overlying the N- regions 22, elevated source/drain 32, and gate electrode 16 in Fig. 7B. The salicide layer 36 is not shown in subsequent figures, but it is to be understood that it may be present.

Fig. 8 illustrates a top view of the gate 16 and elevated source/drain contacts 32. An additional masking process is necessary to remove the polysilicon spacer 32 at the end of the gate 16 in order to separate the source/drain. Fig. 9 illustrates a top view of the gate and source/drain contacts after the polysilicon spacer at the end of the gate 16 has been removed.

The integrated circuit device is completed as is conventional in the art. For example, as illustrated in Fig. 10, insulating layer 50 is deposited over the surface of the substrate. Contact openings are made through the insulating layer to the underlying semiconductor devices, such as to the gate and the elevated source/drain. A metal layer 52 is deposited and patterned to form electrical connections between the elements of the integrated circuit. A passivation layer 54 completes the fabrication of the integrated circuit.

The process of the invention provides a sub-quarter-micron MOSFET device with an elevated source/drain structure having reduced short channel effects. THe use of the polysilcion spacers 32 as an elevated source/drain reduces short channel effects without junction leakage problems presented by shallow source/drain junctions.

While the invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of the invention.

What is claimed is:

1. A method of forming a MOSFET having an elevated source/drain structure in the fabrication of an integrated circuit device comprising:

forming a gate electrode over a gate dielectric on a substrate;

implanting ions into said substrate to form lightly doped regions using said gate electrode as a mask;

thereafter forming dielectric spacers on sidewalls of said gate electrode;

depositing a polysilicon layer overlying said substrate, said gate electrode, and said dielectric spacers wherein said polysilicon layer is heavily doped;

etching back said polysilicon layer to leave polysilicon spacers on said dielectric spacers;

diffusing dopant from said polysilicon spacers into said substrate to form source and drain extension regions underlying said polysilicon spacers; and

removing said polysilicon spacer on an end of said gate electrode to separate said polysilicon spacers into a source polysilicon spacer and a drain polysilicon spacer thereby completing formation of said MOSFET having an elevated source/drain structure in the fabrication of said integrated circuit device.

2. The method according to Claim 1 wherein said step of forming said dielectric spacers comprises:

depositing an oxide layer overlying said semiconductor substrate and said gate electrode; and

etching back said oxide layer to leave said dielectric spacers only on sidewalls of said gate electrode.

3. The method according to Claim 1 wherein said step of forming said dielectric spacers comprises:

oxidizing said semiconductor substrate and said gate electrode to form an oxide layer overlying said semiconductor substrate and said gate electrode; and

etching away said oxide layer overlying said semiconductor substrate and a top surface of said gate electrode to leave said dielectric spacers only on sidewalls of said gate electrode.

4. The method according to Claim 1 wherein said second polysilicon layer is deposited by LPCVD to a thickness of between about 500 and 4000 Angstroms.

5. The method according to Claim 1 wherein said second polysilicon layer is in-situ doped.

6. The method according to Claim 1 wherein said second polysilicon layer is doped by ion implantation.

7. The method according to Claim 1 wherein said second polysilicon layer has a dopant concentration of between about 10^{20} and 10^{22} atoms/cm^3.

8. The method according to Claim 1 wherein said step of diffusing dopant from said polysilicon spacers into said semiconductor substrate to form source and drain regions is performed by a rapid thermal process.

9. A method of forming a MOSFET having an elevated source/drain structure in the fabrication of an integrated circuit device comprising:

forming a gate electrode over a gate dielectric on a substrate;

implanting ions into said substrate to form lightly doped regions using said gate electrode as a mask;

thereafter forming dielectric spacers on sidewalls of said gate electrode;

depositing a polysilicon layer overlying said substrate, said gate electrode, and said dielectric spacers wherein said polysilicon layer is heavily doped;

etching back said polysilicon layer to leave

polysilicon spacers on said dielectric spacers wherein said polysilicon spacers form elevated source/drain regions;

diffusing dopant from said elevated source/drain regions into said substrate to form source and drain extension regions underlying said elevated source/drain regions; and

removing said polysilicon spacer on an end of said gate electrode to separate said elevated source/drain regions into an elevated source region and an elevated drain region thereby completing formation of said MOSFET having an elevated source/drain structure in the fabrication of said integrated circuit device.

10. The method according to Claim 9 wherein said step of forming said dielectric spacers comprises:

depositing an oxide layer overlying said semiconductor substrate and said gate electrode; and

etching back said oxide layer to leave said dielectric spacers only on sidewalls of said gate electrode.

11. The method according to Claim 9 wherein said step of forming said dielectric spacers comprises:

oxidizing said semiconductor substrate and said

gate electrode to form an oxide layer overlying said semiconductor substrate and said gate electrode; and

etching away said oxide layer overlying said semiconductor substrate and a top surface of said gate electrode to leave said dielectric spacers only on sidewalls of said gate electrode.

12. The method according to Claim 9 wherein said second polysilicon layer is in-situ doped.

13. The method according to Claim 9 wherein said second polysilicon layer is doped by ion implantation.

14. The method according to Claim 9 wherein said second polysilicon layer has a dopant concentration of between about 10^{20} and 10^{22} atoms/cm^3.

15. The method according to Claim 9 wherein said step of diffusing dopant from said polysilicon spacers into said semiconductor substrate to form source and drain regions is performed by a rapid thermal process.

16. A method of forming a MOSFET having an elevated source/drain structure in the fabrication of an integrated circuit device comprising:

forming a gate electrode over a gate dielectric on a substrate;

implanting ions into said substrate to form lightly doped regions using said gate electrode as a mask;

thereafter depositing a dielectric layer overlying said semiconductor substrate and said gate electrode;

etching back said dielectric layer to leave dielectric spacers only on sidewalls of said gate electrode;

depositing a polysilicon layer overlying said substrate, said gate electrode, and said dielectric spacers wherein said polysilicon layer is heavily doped;

etching back said polysilicon layer to leave polysilicon spacers on said dielectric spacers wherein said polysilicon spacers form elevated source/drain regions;

diffusing dopant from said elevated source/drain regions into said substrate to form source and drain extension regions underlying said elevated source/drain regions; and

removing said polysilicon spacer on an end of said gate electrode to separate said elevated source/drain regions into an elevated source region and an elevated drain region thereby completing formation of said MOSFET having an elevated source/drain structure in the

fabrication of said integrated circuit device.

17. The method according to Claim 16 wherein said second polysilicon layer is in-situ doped.

18. The method according to Claim 16 wherein said second polysilicon layer is doped by ion implantation.

19. The method according to Claim 16 wherein said second polysilicon layer has a dopant concentration of between about 10^{20} and 10^{22} atoms/cm^3.

20. The method according to Claim 16 wherein said step of diffusing dopant from said polysilicon spacers into said semiconductor substrate to form source and drain regions is performed by a rapid thermal process.