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Abstract

A STRUCTURE WITH COMPOSITE FLOATING GATE BY POLY SPACER IN FLASH

A composite floating gate structure in flash memory cells is disclosed. Parallel active regions separated by isolation regions that extend from the surface of a semiconductor region of a substrate into the semiconductor region. A gate dielectric layer is disposed over the active regions. Planar parts of composite floating gates are composed of a first conductive layer and are equally spaced along the active regions where they are disposed over the gate dielectric layer. Spacer like parts of composite floating gates are composed of a second conductive layer and are disposed over the planar parts along both edges of edges planar parts so that sidewalls of the spacer like parts are parallel to the active regions. The spacer like parts and the planar parts compose the composite floating gates. An interlevel dielectric layer is patterned into equally spaced parallel stripes perpendicular to the active regions and each stripe is disposed over the corresponding composite floating gate for each active region. Word lines, which are composed of a third conductive layer, are parallel lines disposed over the interlevel dielectric layer and serve as control gates.

(Fig. 1a)

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