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(54) **Title**: INTEGRATED CIRCUIT WITH PROGRAMMABLE LOGIC ANALYZER, ENHANCED ANALYZING AND DEBUGGING CAPABILITIES AND METHOD

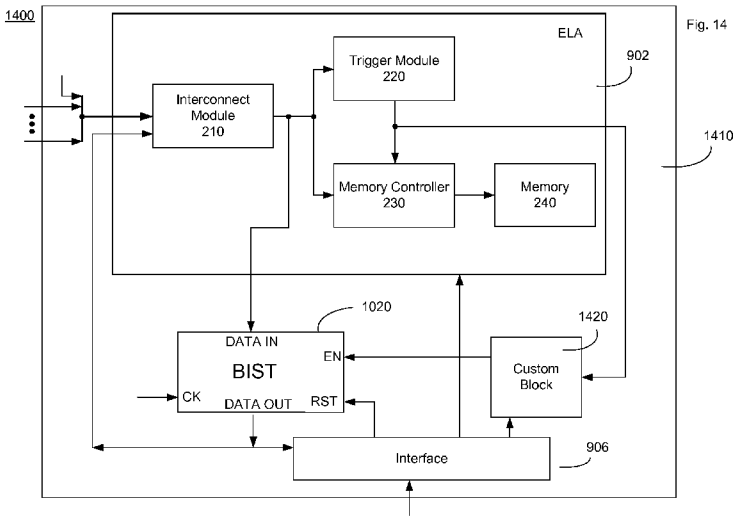

Fig. 14

(57) **Abstract**: An integrated circuit including a logic analyzer with enhanced analyzing and debugging capabilities and a method therefor. In one embodiment, an integrated circuit includes a logic analyzer having a first input receiving a plurality of signals and an output for providing an indication of a detection, by the logic analyzer, of at least one trigger event; and a built in self test block having a first input for receiving one or more of the signals appearing at the first input of the logic analyzer, a second input coupled to the output of the logic analyzer for selectively enabling the BIST block, the BIST block generating and maintaining a signature based upon the first and second inputs thereof.

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