

TIME-WALKING PREVENTION IN A DIGITAL
SWITCHING IMPLEMENTATION FOR CLOCK SELECTION

ABSTRACT OF THE DISCLOSURE

5 A system and method for preventing time-walking
in a digital switching network when switching from a
first clock to a second clock. The first and second
clock can be identical in frequency and independent in
10 phase, where the highest resolution frequency
available is that of said first and second clock. The
system can include a clock divider selection circuit,
an enhanced digital phase aligner, and a clock select
control circuit. The clock divider selection circuit
can output an on-line divided clock and an off-line
15 clock to the enhanced digital phase aligner. The
enhanced digital phase aligner can sample the on-line
divided clock with four phases of the off-line clock
and output an off-line divided clock which is time
shifted such that the off-line divided clock is in
20 phase with the on-line divided clock within plus or
minus one-half the clock period of the off-line clock.
The clock select control circuit can receive the on-
line divided clock from the clock divider selection
circuit, the off-line divided clock from the enhanced
25 digital phase aligner and a smoothed clock. When a
request is made to switch between clock one and clock
two, the clock select control circuit can evaluate the
on-line divided clock and the off-line divided clock
with the smoothed clock and output a clock select
30 control signal to the clock divider selection circuit
based on this comparison.

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