

Description

TECHNICAL FIELD TO WHICH THE INVENTION BELONGS

This invention relates to an IC card according to the preamble of claim 1 and having means for protecting erroneous operation due to incomplete electrical contact with an external power supply.

RELATED BACKGROUND ART

Recently, it has been expected that IC cards are used in many application fields, because of convenience for handling and large memory capacity. The IC cards, which have high security against injustice use by others and can perform various processes by themselves, have been highlighted as a memory medium instead of the magnetic card. The IC cards find many applications for cash cards, personal illness history cards, identification cards, etc.

An IC card is generally made of a plastic card and a semiconductor chip, for example, microcomputer chip and a memory chip sealed in the card. The IC card also has plurality of terminal pads disposed on the surface of the plastic card. The semiconductor chip for IC card is usually a CMOS microcomputer chip which consumes less operational power.

In use, an IC card is inserted into a card reader and then receives a power supply and control signals from the card reader through the terminal pads. Data reception and transmission are carried out between the IC card and the IC card reader.

The document EP-A-0 265 312 describes a known circuit, which prevents writing in a memory of an IC card when the supply voltage is below a threshold value or if the supply line has a high impedance.

A prior art IC card is explained below with reference to Figure 2. The prior art IC cards comprise a microcomputer 100, disposed on a plastic card, terminal pads 10, 11, 12, 13 and 14, resistors R1, R2 and R3, and diodes D1, D2, D3, D4, D5 and D6, as seen Figure 2. The terminal pad 10 receives a positive power supply potential VDD (for example, +5 volts) supplied from the card reader to the microcomputer 100. The terminal pad 11 receives a reset signal RES from the card reader to the microcomputer 100. The terminal pad 12 receives a clock signal CLK from the card reader. The terminal pad 13 receives a serial data SIO from the card reader and transmits a serial data from the microcomputer 100. The terminal pad 14 receives a reference electric potential GND (for example, 0 volts) from the card reader. The protective resistances R1, R2 and R3 are placed between those terminal pads 11, 12 and 13, and the microcomputer. The diodes D1-D6 are connected between the terminal pads 11-13 and the terminal pad 14, forming a protective circuit together with protective resistances R1-

R3. The protective circuit configuration is suitable for protecting the gate insulating layers of a CMOS input circuit I1, I2, I3, (see the Japanese Patent Publication NO. 48-30189).

The above mentioned IC card operates on an external power source supplied through the terminal pads thereof which is contacted mechanically with the terminal pad of the card reader. If incomplete contact between the terminal pads and the card reader occurs, a potential supplied through the reset signal input terminal pad 11, the clock signal input terminal pad 12 and the serial signal terminal pad 13, is supplied to the power supply line through the resistors R1, R2 and R3, and the diodes D1 to D6. The potential is dropped by the protective resistors and the diodes, and is unstable because clock signals are input. However the microcomputer 100 formed of CMOS circuits can incompletely operate on such a dropped voltage. Incomplete contact between terminal pads and a card reader may destroy data stored in an EEPROM or an EPROM in the microcomputer.

The object of the present invention is to solve the above mentioned problems, and particularly to avoid erroneous operation of an IC card due to incomplete electrical contact with an external power supply.

This object is solved by the IC card according to claim 1.

In general, there is provided an IC card having a power supply potential detector, and a reset signal generator to generate a reset signal in response to an output signal receiving signal of the detector.

Particularly, the IC card according to the present invention comprises an IC chip and a plurality of terminal pads located on the surface of the card and being connected to said IC chip, said plurality of terminal pads including a power supply terminal pad, a ground terminal pad, a first signal terminal pad and a second signal terminal pad, the IC card further comprising a potential reducing circuit connected between said power supply terminal pad and said first signal terminal pad; and an erroneous operation protecting circuit comprising a first circuit for detecting incomplete contact between said power supply terminal pad and an external device to output a detecting signal, and a second circuit for generating a reset signal to stop operation of said IC chip in response to said detecting signal, said first circuit including a transistor having a gate electrode receiving a potential on said power supply terminal pad, a source electrode connected to said first signal terminal pad and a drain electrode connected to an input of said second circuit for resetting said IC chip.

The IC card according to the present invention has the advantage that erroneous operation of the IC card can be prevented even if an incomplete contact occurs between terminal pads and an IC card reader.

The erroneous operation protecting circuit preferably further comprises a third circuit having a resistive

potential divider connected between said power supply terminal pad and said ground terminal pad to produce a divided potential, and a transistor having a gate electrode receiving said divided potential, a drain electrode connected to an input of said second circuit, and a source electrode connected to said second signal terminal pad.

The potential reducing circuit preferably comprises a plurality of diodes serially connected.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGURE 1 is a circuit diagram of an IC card having an erroneous operation prevention function according to this invention;

FIGURE 2 is a circuit diagram of a prior art IC card;

FIGURE 3 is a waveform diagram at various nodes of a positive power supply potential detector for an IC card according to this invention;

FIGURE 4 is a waveform diagram at various nodes of a ground potential detector for an IC card according to this invention; and

FIGURE 5 is a waveform diagram at various nodes of a reset signal generator for an IC card according to this invention.

DESCRIPTION OF SPECIAL EMBODIMENT

In Figure 1, an IC card comprises a microcomputer 100, protective resistors R1, R2, and R3, protective diodes reversely connected D2, D4 and D6, and an erroneous operation protecting (preventive) circuit. A power supply terminal pad 10 is provided with a positive potential VDD of +5 volts from an external card reader. A reset signal input terminal pad 11 is provided with a reset signal RES from the card reader which initializes the microcomputer 100. A clock signal input terminal pad 12 is provided with a clock signal CLK from the card reader. A terminal pad 13 relays data S10 in a serial form between the microcomputer 100 and the card reader. A ground terminal pad is provided with a potential GND of 0 volts from the card reader. The protective resistor R1 is coupled between the terminal pad 11 and the gate electrode in a CMOS input circuit I1 of the microcomputer 100, and R2 between the terminal pad 12 and a gate electrode in the CMOS input circuit I2 of the microcomputer 100, and R3 between the terminal pad 13 and the gate electrode in the CMOS input circuit I3 of the microcomputer 100. A potential reducing circuit D11 is coupled between the power supply terminal pad 10 and the gate electrode of the CMOS input circuit I1. The potential reducing circuit D11 is formed of diodes D11a and D11b serially connected, the cathode being connected to the power supply terminal pad 10, and the anode being connected to the gate electrode of the CMOS input circuit I1. A protective diode D2 is coupled be-

tween the gate electrode of the CMOS input circuit I1 and the ground terminal pad 14, the cathode being connected to the gate electrode of the CMOS input circuit I1 and the anode being connected to the ground terminal pad 14. An electrostatic breakage preventing circuit for the CMOS input circuit I1 comprises the protective resistor R1, the potential reducing circuit D11, and the protective diode D2. In the same way, an electrostatic breakage preventing circuit for the CMOS input circuit I2 comprises the protective resistor R2, the potential reducing circuit D13, and the protective diode D4. An electrostatic breakage preventing circuit for CMOS input circuit I3 comprises the protective resistor R3, the potential reducing circuit D15, and the protective diode D6.

An erroneous operation preventing circuit comprises the potential reducing circuits D11, D13 and D15, a ground potential detector 20, a power supply potential detector 30, and a reset signal generator 40.

The ground potential detector 20 comprises a potential dividing resistive circuit, an N-channel transistor T25 a resistor R23 and a capacitor C26. The potential dividing resistive circuit comprises resistors R21 and R22 serially connected between the power supply terminal pad 10 and the ground terminal pad 14. The drain electrode of an N-channel transistor T25 is connected to the power supply terminal pad 10 through the resistor R23, the source electrode is connected to the clock signal input terminal pad 12 through the resistor R2 and the gate electrode is connected to the node N24 of the potential dividing resistive circuit. The capacitor C26 is connected parallelly to the resistor R22.

The ground potential detector 20 detects a potential more than zero volts at the ground terminal pad 14, and outputs a detecting signal from the drain of the transistor T25 to the reset signal generator 40. The power supply potential detector 30 comprises a protective N-channel transistor T32, a resistor R31 and a P-channel transistor T33. The protective N-channel transistor T32 has the drain electrode connected to the power supply terminal pad 10 through the resistor 31, and both the source electrode and the gate electrode connected to the ground terminal pad 14. The P-channel transistor T33 has the drain electrode connected to the node N33, the source electrode connected to the reset signal input terminal pad 11 through the resistor R1, gate electrode connected to the drain of the protective transistor T32. The power supply potential detector 30 detects a potential less than a power supply potential (for example +5 volts) and outputs a detecting signal from the drain of transistor T33 to the reset signal generator 40.

The reset signal generator 40 comprises inverters I41, I42, an OR gate G43 and a R/S flipflop 44. The reset signal input terminal of the R/S flipflop 44 is connected to the reset signal input terminal pad 11 through the resistor R1 through the inverter I41, and

the set terminal is connected to the output of the OR gate G43. The OR gate G43 is connected to an output signal of the ground potential detector 20 through the inverter I42 and to the node N33 of the power supply potential detector 30. The reset signal generator 40 is initialized by the reset signal received at the terminal pad 11, and outputs the reset signal to the microcomputer by receiving an output signal of the ground potential detector 20 or the power supply potential detector 30.

Next, operation of an erroneous operation prevention circuit suitable for an IC card according to this invention is explained below.

Let us assume that the power supply terminal pad 10 is incompletely contacted to an external card reader, but both the reset signal input terminal pad 11 and the ground terminal pad 14 are in contact with the card reader to be provided with +5 volts and 0 volts, respectively.

In this case, the power supply potential detector 30 detects incomplete contact between the power supply terminal pad 10 and the card reader. The power supply potential detector 30 operates in accordance with the waveforms shown in FIGURE 3.

A potential of 4 volts appears at the power supply terminal pad 10 in spite of the defective contacts between the power supply terminal pad 10 and the card reader, since the potential reducing circuit D11 decreases the power supply potential (5 volts).

The power supply terminal pad 10 is at 4 volts and the source electrode of the P-channel transistor T33 is at +5 volts, and the drain electrode of the protective transistor T32 is at 0 volts. The protective transistor T32, an N-channel transistor, is in off state. The protective circuit for the P-channel transistor T33 consists of the protective transistor T32 and the resistor R31. Since the potential of the gate electrode receives 4 volts, the P-channel transistor T33 turns on to output an "H" level signal to the reset signal generator 40. This means that the potential at the gate electrode of the P-channel transistor T33 is less than that of the reset signal input terminal pad 11. For this reason, the power supply potential detector 30 also can detect an sudden drop in voltage at the power supply terminal pad 10, even if the terminal pad 10 is completely contacted to the external card reader.

In case both the power supply terminal pad 10 and clock signal input terminal pad 12 are completely contacted to the card reader to receive +5 volts and a clock signal having a swing of 0 to +5 volts, respectively, while the ground terminal pad 14 is incompletely contacted to the card reader, the ground potential detector 20 detects incomplete contact between the ground terminal pad 14 and the card reader.

The ground potential detector 20 operates in accordance with the waveforms shown in FIGURE 4. When the clock signal terminal pad 12 is in an "L" level, the ground terminal pad 14 becomes 0.5 volts. In

the ground potential detector 20, the substrate potential of the N-channel transistor T25 is 0.5 volts and the source electrode potential of the N-channel transistor T25 is 0 volts. The resistance ratio of the resistors R21 and R22 are selected in that the transistor T25 turns on when the ground terminal pad 14 is in the uncontact condition, and it does not turn on when the ground terminal pad 14 is in the contact condition. Preferably, the resistance ratio is 9:1, which turns the transistor T25 on to output an "L" level signal to the reset signal generator 40 when the ground terminal pad 14 rises to about 0.5 volts. The capacitor C26 bypasses a potential rise on the ground terminal pad 14 due to noise to prevent the ground potential detector 20 from unnecessarily outputting a detecting signal.

The ground potential detector 20 can output a detecting signal when the potential of the ground terminal pad 14 rises the threshold potential of a diode.

The reset signal generator 40 sends a reset signal to the microcomputer chip 100 in response to a detecting signal from the ground potential detector 20 or the power supply potential detector 30.

The reset signal generator 40 operates in accordance with waveforms showing in FIGURE 5.

The R/S flipflop 44 is reset in response to a reset signal on the reset signal input terminal pad 11. Then, the R/S flipflop 44 receives a detecting signal from OR gate G43 to output a reset signal of an "H" level signal to the microcomputer 100.

As a result, the reset signal generator 40 continues to send a reset signal to stop operation of the microcomputer 100 while an IC card and an external card reader are in uncontact condition.

INDUSTRIAL APPLICABILITY

The IC cards according to this invention are applied for many applications, such as cash cards, personal illness history cards, identification cards, etc.

Claims

1. An IC card having an IC chip (100) and a plurality of terminal pads (10 to 14) located on the surface of the card and being connected to said IC chip, said plurality of terminal pads including a power supply terminal pad (10), a ground terminal pad (14), a first signal terminal pad (11) and a second signal terminal pad (12), the IC card further comprising a potential reducing circuit (D11) connected between said power supply terminal pad (10) and said first external signal terminal, pad (11), characterized by: an erroneous operation protecting circuit (20,30,40) comprising a first circuit (30) for detecting incomplete contact between said power supply terminal pad (10) and an external device to output a detecting signal, and a sec-



the set terminal is connected to the output of the OR gate G43. The OR gate G43 is connected to an output signal of the ground potential detector 20 through the inverter I42 and to the node N33 of the power supply potential detector 30. The reset signal generator 40 is initialized by the reset signal received at the terminal pad 11, and outputs the reset signal to the microcomputer by receiving an output signal of the ground potential detector 20 or the power supply potential detector 30.

Next, operation of an erroneous operation prevention circuit suitable for an IC card according to this invention is explained below.

Let us assume that the power supply terminal pad 10 is incompletely contacted to an external card reader, but both the reset signal input terminal pad 11 and the ground terminal pad 14 are in contact with the card reader to be provided with +5 volts and 0 volts, respectively.

In this case, the power supply potential detector 30 detects incomplete contact between the power supply terminal pad 10 and the card reader. The power supply potential detector 30 operates in accordance with the waveforms shown in FIGURE 3.

A potential of 4 volts appears at the power supply terminal pad 10 in spite of the defective contacts between the power supply terminal pad 10 and the card reader, since the potential reducing circuit D11 decreases the power supply potential (5 volts).

The power supply terminal pad 10 is at 4 volts and the source electrode of the P-channel transistor T33 is at +5 volts, and the drain electrode of the protective transistor T32 is at 0 volts. The protective transistor T32, an N-channel transistor, is in off state. The protective circuit for the P-channel transistor T33 consists of the protective transistor T32 and the resistor R31. Since the potential of the gate electrode receives 4 volts, the P-channel transistor T33 turns on to output an "H" level signal to the reset signal generator 40. This means that the potential at the gate electrode of the P-channel transistor T33 is less than that of the reset signal input terminal pad 11. For this reason, the power supply potential detector 30 also can detect an sudden drop in voltage at the power supply terminal pad 10, even if the terminal pad 10 is completely contacted to the external card reader.

In case both the power supply terminal pad 10 and clock signal input terminal pad 12 are completely contacted to the card reader to receive +5 volts and a clock signal having a swing of 0 to +5 volts, respectively, while the ground terminal pad 14 is incompletely contacted to the card reader, the ground potential detector 20 detects incomplete contact between the ground terminal pad 14 and the card reader.

The ground potential detector 20 operates in accordance with the waveforms shown in FIGURE 4. When the clock signal terminal pad 12 is in an "L" level, the ground terminal pad 14 becomes 0.5 volts. In

the ground potential detector 20, the substrate potential of the N-channel transistor T25 is 0.5 volts and the source electrode potential of the N-channel transistor T25 is 0 volts. The resistance ratio of the resistors R21 and R22 are selected in that the transistor T25 turns on when the ground terminal pad 14 is in the uncontact condition, and it does not turn on when the ground terminal pad 14 is in the contact condition. Preferably, the resistance ratio is 9:1, which turns the transistor T25 on to output an "L" level signal to the reset signal generator 40 when the ground terminal pad 14 rises to about 0.5 volts. The capacitor C26 bypasses a potential rise on the ground terminal pad 14 due to noise to prevent the ground potential detector 20 from unnecessarily outputting a detecting signal.

The ground potential detector 20 can output a detecting signal when the potential of the ground terminal pad 14 rises the threshold potential of a diode.

The reset signal generator 40 sends a reset signal to the microcomputer chip 100 in response to a detecting signal from the ground potential detector 20 or the power supply potential detector 30.

The reset signal generator 40 operates in accordance with waveforms showing in FIGURE 5.

The R/S flipflop 44 is reset in response to a reset signal on the reset signal input terminal pad 11. Then, the R/S flipflop 44 receives a detecting signal from OR gate G43 to output a reset signal of an "H" level signal to the microcomputer 100.

As a result, the reset signal generator 40 continues to send a reset signal to stop operation of the microcomputer 100 while an IC card and an external card reader are in uncontact condition.

INDUSTRIAL APPLICABILITY

The IC cards according to this invention are applied for many applications, such as cash cards, personal illness history cards, identification cards, etc.

Claims

1. An IC card having an IC chip (100) and a plurality of terminal pads (10 to 14) located on the surface of the card and being connected to said IC chip, said plurality of terminal pads including a power supply terminal pad (10), a ground terminal pad (14), a first signal terminal pad (11) and a second signal terminal pad (12), the IC card further comprising a potential reducing circuit (D11) connected between said power supply terminal pad (10) and said first external signal terminal, pad (11), characterized by: an erroneous operation protecting circuit (20,30,40) comprising a first circuit (30) for detecting incomplete contact between said power supply terminal pad (10) and an external device to output a detecting signal, and a sec-



ond circuit (40) for generating a reset signal (RESET) to stop operation of said IC chip (100) in response to said detecting signal, said first circuit (30) including a transistor (T33) having a gate electrode receiving a potential (VDD) on said power supply terminal pad (10), a source electrode connected to said first signal terminal pad (11) and a drain electrode connected to an input of said second circuit (40) for resetting said IC chip.

2. An IC card according to claim 1, wherein said erroneous operation protecting circuit further comprises a third circuit (20) having a resistive potential divider (R21, R22) connected between said power supply terminal pad (10) and said ground terminal pad (14) to produce a divided potential, and a transistor (T25) having a gate electrode receiving said divided potential, a drain electrode connected to an input of said second circuit (40), and a source electrode connected to said second signal terminal pad (12).
3. An IC card according to claim 1, wherein said potential reducing circuit (D11) comprises a plurality of diodes (D11a, D11b) serially connected.

Patentansprüche

1. IC-Karte mit einem IC-Chip (100) und einer Vielzahl von Anschlußflecken (10 bis 14), die sich auf der Oberfläche der Karte befinden und die mit dem IC-Chip verbunden sind, wobei die Vielzahl von Anschlußflecken einen Stromversorgungs-Anschlußfleck (10), einen Erdanschlußfleck (14), einen ersten Signalanschlußfleck (11) und einen zweiten Signalanschlußfleck (12) umfaßt und wobei die IC-Karte weiterhin eine Potentialreduzierschaltung (D11) aufweist, die zwischen dem Stromversorgungs-Anschlußfleck (10) und dem ersten Signalanschlußfleck (11) verbunden ist, gekennzeichnet durch: eine Fehlbetriebs-Schutzschaltung (20, 30, 40), die eine erste Schaltung (30) zum Nachweis eines mangelhaften Kontakts zwischen dem Stromversorgungs-Anschlußfleck (10) und einem externen Gerät, um ein Nachweissignal auszugeben, und eine zweite Schaltung (40) zur Erzeugung eines Rücksetzsignals aufweist, um als Antwort auf das Nachweissignal den Betrieb des IC-Chips (100) anzuhalten, wobei die erste Schaltung (30) einen Transistor (T33) mit einer Gate-Elektrode, die ein Potential (VDD) auf dem Stromversorgungs-Anschlußfleck (10) empfängt, eine Source-Elektrode, die mit dem ersten Signalanschlußfleck (11) verbunden ist, und eine Drain-Elektrode umfaßt, die mit einem Eingang der zweiten Schaltung (40) zum Rücksetzen des IC-

Chips verbunden ist.

2. IC-Karte nach Anspruch 1, wobei die Fehlbetriebs-Schutzschaltung weiterhin eine dritte Schaltung (20), die einen Widerstands-Potentialteiler (R21, R22) aufweist, der zwischen dem Stromversorgungs-Anschlußfleck (10) und dem Erdanschlußfleck (14) verbunden ist, um ein Zweigpotential zu erzeugen, und einen Transistor (T25) umfaßt, der eine Gate-Elektrode, die das Zweigpotential empfängt, eine Drain-Elektrode, die mit einem Eingang der zweiten Schaltung (40) verbunden ist, und eine Source-Elektrode aufweist, die mit dem zweiten Signalanschlußfleck (12) verbunden ist.
3. IC-Karte nach Anspruch 1, wobei die Potentialreduzierschaltung (D11) eine Vielzahl von hintereinander verbundenen Dioden (D11a, D11b) umfaßt.

Revendications

1. Carte à circuit intégré comprenant une puce à circuit intégré (100) et une pluralité de plots de connexion (10 à 14) situés sur la surface de la carte et étant connectés à ladite puce à circuit intégré, ladite pluralité de plots de connexion comportant un plot de connexion de source d'alimentation (10), un plot de connexion de masse (14), un premier plot de connexion de signaux (11) et un second plot de connexion de signaux (12), la carte à circuit intégré comprenant en outre un circuit (D11) réducteur de potentiel connecté entre ledit plot de connexion de source d'alimentation (10) et ledit premier plot de connexion de signaux externes (11), caractérisée par un circuit (20, 30, 40) de protection contre un fonctionnement erroné comprenant un premier circuit (30) pour détecter un contact incomplet entre ledit plot de connexion de source d'alimentation (10) et un dispositif extérieur afin de délivrer un signal de détection, et un second circuit (40) pour générer un signal de remise à l'état initial (RESET) afin d'arrêter le fonctionnement de ladite puce à circuit intégré (100) en réponse audit signal de détection, ledit premier circuit (30) comportant un transistor (T33) ayant une électrode de grille recevant un potentiel (VDD) sur ledit plot de connexion de source d'alimentation (10), une électrode de source connectée audit premier plot de connexion de signaux (11) et une électrode de drain connectée à une entrée dudit second circuit (40) pour remettre à l'état initial ladite puce à circuit intégré.
2. Carte à circuit intégré selon la revendication 1,



dans laquelle ledit circuit de protection contre un fonctionnement erroné comporte en outre un troisième circuit (20) ayant un diviseur de potentiel résistif (R21, R22) connecté entre ledit plot de connexion de source d'alimentation (10) et ledit plot de connexion de masse (14) pour produire un potentiel divisé, et un transistor (T25) ayant une électrode de grille recevant ledit potentiel divisé, une électrode de drain connectée à une entrée dudit deuxième circuit (40), et une électrode de source connectée audit second plot de connexion de signaux (12).

5

10

3. Carte à circuit intégré selon la revendication 1, dans laquelle ledit circuit (D11) réducteur de potentiel comporte une pluralité de diodes (D11a, D11b) connectées en série.

15

20

25

30

35

40

45

50

55

6