

The invention is based on a circuit arrangement for producing a clock signal coupled to the line frequency for decoding digitalised television signals by using a first phase-regulated oscillator circuit (PLL) to which is supplied a reference frequency produced with the aid of a second phase-regulated oscillator circuit.

When processing digital signals, particularly when digitalising video signals, the important precondition is that the clock pulse should be coupled to the line frequency both in frequency and in phase position in order to control the digital circuits. Thus it is ensured that both from line to line and from field to field the instantaneous values are formed always at the same points. According to the scanning theorem with a transmission width of 6 MHz the clock pulse frequency is between 10 and 20 MHz. The proposed standard envisages a frequency of 13.5 MHz for this. Synchronisation of the clock pulse frequency may only take place during the non-visible part, during the line return, with the clock oscillator oscillating freely during the forward propagation of the line. If the relationship between the clock and the line frequency is very large and the clock frequency is not sufficiently stable, there is the danger of jittering during the forward propagation of the line, whereby regulation during the line is restricted disadvantageously. If the clock frequency were produced with the aid of a quartz controlled PLL circuit, there would be no possibility of adjustment for changing the frequency, if for example the line frequency deviates from the standard, as is the case with signals from a video recorder. The line frequency may deviate in these devices by $\pm 1\%$. Therefore, setting the clock frequency has to be possible in order that it is synchronous to the line frequency of the signal to be processed, in order to avoid jitter.

For example it has been proposed to produce the required clock frequency with the aid of a quartz controlled PLL circuit, while the clock frequency is obtained by dividing and then multiplying (IEEE International Conference on Consumer Electronics, 7.6.85, Session XVII Digital T.V.). However this is connected with a large cost on circuitry.

In US-A 4463371 a circuit arrangement is shown which serves to decode digitalised television signals, in which the clock frequency is produced with the aid of a PLL circuit. Associated with this PLL circuit is a second PLL circuit which produces the reference frequency for the first PLL circuit. This reference frequency is coupled to the burst signal of the colour

signal. This burst signal does however have a high frequency of 4.43 MHz, an expensive quartz (clock) being necessary for producing it as a reference frequency.

The object underlying the invention is to produce at low circuit cost a clock frequency coupled to the line frequency of a video signal, the value of which is automatically adapted to the current line frequency which has tolerances. This object is achieved by the teaching provided in the patent claim. Further advantageous refinements of the invention are described in the dependent claims.

The essentials of the invention are explained below together with an embodiment with the aid of the drawings.

In order to produce the clock frequency f_T at the output 0 there is a PLL circuit which consists of a voltage controlled oscillator 1, a frequency divider 2 and a phase comparator 3. In a manner known per se the divided frequency f_T/N_1 and a reference frequency f_R are supplied to the phase comparator 3. From phase comparison a control voltage for the oscillator 1 results. The reference frequency f_R is produced with the aid of a second PLL circuit which consists of a second voltage-controlled oscillator 4, a second frequency divider 5 and a second phase comparator 6. This second PLL circuit produces the frequency f_R which is firmly coupled to the line frequency f_Z . The line frequency f_Z and the subdivided frequency f_R/N_2 is fed as the reference frequency to the phase comparator 6. Through the ceramics oscillator 9 the oscillator 4 delivers a very stable frequency f_R for the first PLL circuit. The first oscillator 1, which delivers a clock frequency of 13.5 MHz for example is regulated with the aid of the reference frequency of 500 kHz. Due to the small frequency ratio $f_T/f_R < 100$ high stability is ensured. The time constant T_2 of the second PLL circuit 4, 5, 6, given by the capacitor 8, is greater than the time constant T_1 of the first PLL circuit 1, 2, 3, given by the capacitor 7. Thus it is advantageous if time constant T_2 of the PLL circuit 4, 5, 6 is of the order of magnitude of five to twenty periods of the line frequency. With a line frequency of 15,625 KHz the value for T_2 is then at 320 μs to 1280 μs . The time constant T_1 of the PLL circuit 1, 2, 3 is then lower in relation to the factor N_2 of the frequency divider 5. In the example mentioned with $N_2 = 32$ the value for the time constant T_1 is between 10 μs and 40 μs . The capture range of the second PLL circuit 4, 5, 6 can be small due to the ceramics oscillator 9. Since the first PLL circuit has a smaller time constant T_1 , a normal voltage-controlled

oscillator may be used without recourse to an expensive oscillating element (e.g. ceramic or quartz). The first oscillator 1 therefore does not need to be settable from outside either, because the reference frequency f_R fed to the first PLL circuit changes according to the deviations in the line frequency f_Z .

In order to produce a clock frequency of for example 13.5 MHz the second oscillator 4 is set to 500 kHz with the aid of a ceramics oscillator oscillating to 503 kHz, while said frequency divided by the factor $N_2 = 32$ is compared with the line frequency $f_Z = 15,625$ KHz. The reference frequency f_R thus produced is compared with the frequency f_T divided by the factor $N_1 = 27$. The reference frequency f_R will always be set during deviation in the line frequency by $\pm 1\%$ such that it produces a clock frequency of 13.5 MHz in the first PLL circuit.

The invention is particularly well suited to producing a stable clock frequency for decoding video text signals. An expensive quartz is thus saved. The exact line frequency of the television transmitter is used as a reference frequency. The use of a ceramic oscillator allows sufficient freedom from faults.



Patent Claims

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1. A circuit arrangement for producing a clock signal coupled to a television signal, for decoding digitalised television signals while using a first phase-regulated oscillator circuit (PLL) to which is supplied a reference frequency produced with the aid of a second phase-regulated oscillator circuit, characterised in that the clock signal is coupled to the line frequency (f_Z) which may have a deviation of $\pm 1\%$, and that the reference frequency (f_R) for the first phase-regulated oscillator circuit (1,2,3) is a whole-numbered multiple of the line frequency (f_Z) of the television signals and the ratio between the clock signal frequency (f_T) and the reference frequency (f_R) is less than 100 and that the time constant (T_2) of the regulating circuit of the second phase-regulated oscillator circuit is greater than the time constant (T_1) of the regulating circuit of the first phase-regulated oscillator circuit and that the capture range for the second phase-regulated oscillator circuit is smaller than the capture range for the first phase-regulated oscillator circuit and that the first phase-regulated oscillator circuit has a ceramics oscillator.
2. A circuit arrangement according to claim 1, characterised in that the digitalised television signals are video text signals.
3. A circuit arrangement according to claim 1 or 2, characterised in that the first phase-regulated oscillator circuit includes a first frequency divider (2) with the divider factor $N_1 = 27$ and the second phase-regulated oscillator circuit



includes a second frequency divider (5) with the divider factor $N_2 = 32$ and that the time constant (T_2) of the regulating circuit of the second phase-regulated oscillator circuit is in the region of 5 to 20 periods of the line frequency (f_z).