Abstract

COMPUTER SYSTEM

A computer system is provided having apparatus (11) between a central processing unit (CPU) (19) and a peripheral device (15) which ensures compatibility between existing software for the peripheral device (15) and a CPU (19) of any speed. The apparatus (11) waveshapes read or write strobe signals in a transfer cycle between the peripheral device and the CPU (19) in order to ensure timing parameters of the peripheral device (15) are not violated by fast CPUs. If the waveshaping causes a change in the timing between first and second consecutive read or write strobe signals, the interface (11) provides a wait signal to the CPU for the purpose of instructing it to extend the transfer cycle of the second strobe signal. In the illustrated embodiment, an apparatus (11) according to the invention is part of a video subsystem connecting a microprocessor unit (MPU) (19) and a video digital-to-analog converter (video DAC) (15). Writing or reading color data to or from the video DAC occurs by way of the apparatus (11) of the invention. The MPU (19) is slowed while it writes or reads color data only when it is required to prevent violation of the timing parameters of the video DAC (15). In this regard, slower MPUs are not penalized by the invention since wait states are inserted into a transfer cycle only when it is necessary to re-space consecutive read or write strobe signals to prevent the violation of timing parameters.

This Sheet Has Been Replaced

