additional deposition process may be required to properly compensate for wafer bow after the internal stress of the prior backside films shifts during an operation that anneals the backside films. This adds complexity to device manufacturing and decreases overall throughput.

BACKSIDE FILM INTERNAL STRESS SHIFT COMPENSATION

[0036] Disclosed herein are methods, systems, and techniques for maintaining the internal stress of backside layers deposited at low temperature deposition conditions and subsequently annealed at high temperatures. This reduces the need for additional backside film deposition, reduces the risk of a wafer handling problem during subsequent wafer processing, and maintains wafer bow compensation after annealing without cracking of the backside films.

[0037] Figure 2A and 2B illustrate layers having a tensile stress shift and a compressive stress shift, respectively. In Figure 2A, a substrate 200 has a tensile stress shift layer 211a having an internal tensile stress (hence the "bowl" shape). A wafer bow 203 is shown as a deflection from the center to edge of the substrate, and may be measured along an axis normal to a plane tangent to the minima of the curve of the wafer (i.e., solid line shown). Following a thermal cycle, annealed tensile stress shift layer 211a has cracked, as shown by cracked layer 211b having cracks 213. As a result, substrate 200a may have a lower wafer bow 204a as the cracked layer 211b has reduced its internal stress by a cracking failure. In some embodiments, cracking may not necessarily affect wafer bow, e.g., wafer bow 204a may be much closer to or the same as wafer bow 203, but cracking may cause defects and compromise the film integrity. For example, during a downstream wet chemistry process, species may diffuse into the cracks and cause undesirable reactions.

[0038] In Figure 2B, substrate 200 has a compressive stress shift layer 215a having an internal tensile stress and wafer bow 203, similar to Figure 2A. After a thermal cycle, annealed compressive stress shift layer 215b has a lower internal tensile stress and thus a reduced wafer bow 204b for substrate 200b. In both Figure 2A and 2B, the internal stress shift following annealing has reduced the ability of the backside films to counteract wafer bow. It should be understood that for both Figures 2A and 2B (and also 2C) that greater wafer bow is indicative of a greater ability of the backside film to counteract wafer bow from frontside layers. Backside films may be deposited on flat wafers and the resulting wafer bow indicates how much wafer bow the backside films may counteract when deposited on substrates having frontside layers that cause bowing and are thus already bowed.

[0039] To address this concern, in some embodiments a combination of compressive stress shift and tensile stress shift layers may be deposited. By depositing both types of layers, the wafer bow may be properly compensated for prior and subsequent to an annealing operation,

636) and a ShoPed 606. In some embodiments, the gas-flowing pedestal (i.e., ShoPed) is a combination showerhead and pedestal, which enables deposition on a back-side of the wafer. The electrode geometry combines features of a showerhead, e.g., a gas mixing plenum, holes, hole-pattern, gas jet preventing baffle, and features of a pedestal. Examples of features of a pedestal include an embedded controlled heater, wafer-lift mechanisms, ability to hold plasma suppression rings, and movability. This enables the transfer of wafers and the processing of gasses with or without RF power from the pedestal.

[0076] In some embodiments, the system may have a wafer lift mechanism that tightly controls parallelism of the substrates against the electrodes. In one example, this may be achieved by setting up the lift mechanism parallel to the two electrodes and controlling manufacturing tolerances, e.g., spindle or lift pins mechanisms. In another example, the lift may be achieved by raising the wafer lift parts. This option may not allow dynamic control of the side that gets deposited.

[0077] In some configurations, the lift mechanism may allow dynamically controlling the substrate position during processing (before plasma, during plasma, after plasma) to control the side of the deposition, profile of the deposition, and deposition film properties. The system may further allow selective enabling/disabling of the side where reactants are flown. One side can flow the reactant and the other side can flow inert gases to suppress the deposition and plasma.

[0078] In some embodiments, the gap between the side of the wafer that does not need plasma/dep may be tightly controlled. This distance may be controlled to suppress plasma. By not controlling the distance, the wafer may be susceptible to plasma damage. For example, the system may allow a minimal gap from about 2 mm to about 0.5 mm, and in another embodiment from about 1 mm to about .05 (limited by the wafer bow), and such gap can be controlled. The gap maybe controlled depending on process conditions.

[0079] In some embodiments, the gas-flowing pedestal (i.e., ShoPed) may enable, without limitation: (a) thermal stabilization of the wafer to processing temperature prior to processing; (b) selective design of hole patterns on the ShoPed to selectively deposition film in different areas of the back-side of the wafer; (c) swappable rings can be attached to achieve appropriate plasma confinement and hole pattern; (d) stable wafer transfer mechanisms within chamber and for transferring wafer outside to another chamber or cassette – such as lift pins, RF-coupling features, minimum-contact arrays; (e) implement gas mixing features, e.g., such as inner plenum, baffle and manifold lines openings; and (f) add compartments in the gas-flowing

pedestal (i.e., ShoPed) to enable selective gas flow to different regions of the back side of the wafer and control flow rates via flow controllers and/or multiple plenums.

[0080] In another embodiment, dynamic gap control using wafer lift mechanism enables: (a) control of the distance from deposition or reactant flowing electrode to the side of the wafer that needs deposition or in the middle so that both sides can be deposited; and (b) the lift mechanism to control the distance dynamically during the process (before plasma, during plasma, after plasma) to control the side of the deposition, profile of the deposition, and deposition film properties. In another embodiment, for a deposition mode used to deposit on the backside of the wafer, film edge exclusion control is highly desirable to avoid lithography-related overlay problems. The lift mechanism used in this system is done via a carrier ring 654 that has a design feature to shadow the deposition on the edge. This specifies the edge exclusion control via the design and shape of the carrier ring.

[0081] Figure 7A shows a cross-sectional view of an edge region of the ShoPed 606. This view provides a cross-sectional representation of the carrier ring 654, which has a carrier ring inner radius 654a and a carrier ring outer radius 654b. In some embodiments, the carrier ring 654 includes support extensions 654c, which extend below the substantial flat surface of the carrier ring 654.

[0082] The support extensions 654c are configured to mate and sit within support surfaces defined into a top surface of the spacers 644. The support surfaces provide a complementary mating surface for the support extensions 654c, such that the carrier ring 654 is prevented from sliding or moving when supported by the spacers 644. Although three spacers are shown as spacers 644 are shown in Figure 7B, it is envisioned that any number of spacers may be provided, so long as the carrier ring can be supported substantially parallel to the surface of the ShoPed 606, and spacing is defined for supporting wafer 602 at a spaced apart relationship from a top surface of the ShoPed 606.

[0083] Further shown is that a top surface of the ShoPed 606 will include a hole pattern 606a that is distributed throughout the surface to provide even distribution and output of gases during operation. In one embodiment, the hole pattern 606a is distributed in a plurality of concentric rings that start at the center of the top surface of the ShoPed 606 and extend to an outer periphery of the ShoPed 606. At least one hole pattern 606a is provided at an edge hole region 607 of the hole pattern, and orifices defined in the edge hole region 607 are preferably angled to provide gases non-perpendicular to the surface of the ShoPed 606.

[0084] In one example, the angle or tilt at which the orifices in the edge hole region 607 is defined to tilt or angle away from the center of the ShoPed 606. In one embodiment, the angle

is approximately 45° from horizontal. In other embodiments, the angle can vary between 20° from horizontal to about 80° from horizontal. In one embodiment, by providing the angled orifices in the edge hole region 607, additional distribution of process gases can be provided during backside deposition of the wafer 602. In one embodiment, the remainder orifices 606d of the hole pattern 606a are oriented substantially perpendicular to the surface of the ShoPed 606 and directed toward the underside of the wafer 602.

[0085] Figure 7B illustrates that when the wafer 602 is held by the carrier ring 654, the wafer 602 edge will sit on an edge region closer to the carrier ring inner radius 654a of the carrier ring 654. The surface of the showerhead 636 facing the top surface of the wafer 602, when positioned using spacers 644, may be substantially close to prevent deposition during a mode where deposition is being carried out to the backside of the wafer 602.

[0086] By way of example, the distance between the top of the wafer 602 and the surface of the showerhead 636 is preferably between about 2 mm to about.5 mm, and in some embodiments about 1 mm to about .5 mm, depending on the wafer bow. That is, if the wafer is bowed substantially, the separation will be about .5 mm or larger. If the wafer is not yet bowed substantially, the separation can be less than about .5 mm. In one embodiment, it is preferable that the separation be minimized to prevent deposition on the top side of the substrate when the backside of the substrate is being deposited with a layer of material. In some embodiments, the showerhead 636 is configured to supply an inert gas flow over the top side of the wafer 602 during when the backside of the substrate is being deposited and deposition gases are being supplied by the ShoPed 606.

[0087] Any suitable chamber may be used to implement the disclosed embodiments. Example deposition apparatuses include various systems, e.g., ALTUS® and ALTUS® Max, available from Lam Research Corp., of Fremont, California, or any of a variety of other commercially available processing systems.

[0088] Figure 8 is a schematic of a process system suitable for conducting deposition processes, such as frontside deposition processes, in accordance with embodiments. The system 800 includes a transfer module 803. The transfer module 803 provides a clean, pressurized environment to minimize risk of contamination of substrates being processed as they are moved between various reactor modules. Mounted on the transfer module 803 is a multi-station reactor 809 capable of performing ALD, treatment, and CVD according to various embodiments. Multi-station reactor 809 may include multiple stations 811, 813, 815, and 817 that may sequentially perform operations in accordance with disclosed embodiments. Stations

CLAIMS

1. A method of reducing bow in a substrate, the method comprising:

receiving a substrate having one or more frontside layers on a frontside of the substrate, wherein the one or more frontside layers induce a bow in the substrate;

depositing a first backside layer, wherein the first backside layer has a first type of internal stress shift after annealing;

depositing a second backside layer, wherein the second backside layer has a second type of internal stress shift after annealing that is opposite the first type of internal stress shift.

2. The method of claim 1, wherein the first backside layer comprises more silicon-hydrogen bonds than the second backside layer.

3. The method of claim 1, further comprising annealing the substrate, wherein a combined internal stress of the first backside layer and the second backside layer changes by less than 10% after annealing.

4. The method of claim 3, wherein annealing occurs at a temperature greater than about 700 °C.

5. The method of claim 1, wherein depositing the first backside layer and depositing the second backside layer are performed at temperatures less than about 500°C.

6. The method of claim 1, wherein the first type of internal stress shift is a tensile stress shift.

7. The method of claim 6, wherein the second type of internal stress shift is a compressive stress shift.

8. The method of claim 1, wherein the first backside layer and second backside layer both have a tensile internal stress.

9. A substrate comprising:

one or more frontside layers on a frontside of the substrate;

a first backside layer, wherein the first backside layer has a first type of internal stress shift after annealing;

a second backside layer, wherein the second backside layer has a second type of internal stress shift after annealing that is opposite the first type of internal stress shift.

10. The substrate of claim 9, wherein, if from the one or more frontside layers are not compensated by the first backside layer, the substrate has a bow of about 300 μm or more.

11. The substrate of claim 9, wherein the first type of internal stress shift is tensile and the second type of stress shift is compressive.

12. The substrate of claim 9, wherein the first backside layer and second backside layer comprise silicon nitride.

13. The substrate of claim 9, wherein the first backside layer comprises more silicon-hydrogen bonds than the second backside layer.

14. An apparatus for semiconductor processing, the apparatus comprising:

a process chamber; and

a controller comprising memory and processors configured for:

receiving a substrate having one or more frontside layers on a frontside of the substrate, wherein the one or more frontside layers induce a bow in the substrate;

depositing a first backside layer, wherein the first backside layer has a first type of internal stress shift after annealing;

depositing a second backside layer, wherein the second backside layer has a second type of internal stress shift after annealing that is opposite the first type of internal stress shift.