A METHOD TO FORM LOW-OVERLAP-CAPACITANCE TRANSISTORS BY FORMING MICROTRENCH AT THE GATE EDGE

ABSTRACT

A method for forming a transistor having low overlap capacitance by forming a microtrench at the gate edge to reduce effective dielectric constant is described. A gate electrode is provided overlying a gate dielectric layer on a substrate and having a hard mask layer thereover. An oxide layer is formed overlying the substrate. First spacers are formed on sidewalls of the gate electrode and overlying the oxide layer. Source/drain extensions are implanted. Second spacers are formed on the first spacers. Source/drain regions are implanted. A dielectric layer is deposited overlying the gate electrode and the oxide layer and planarized to the hard mask layer whereby the first and second spacers are exposed. The exposed second spacers and underlying oxide layer are removed. The exposed substrate underlying the second spacers is etched into to form a microtrench undercutting the gate oxide layer at an edge of the gate electrode. The microtrench is filled with an epitaxial oxide layer and planarized to the hard mask layer. The dielectric layer is patterned to form third spacers on the epitaxial oxide layer. The microtrench reduces the effective dielectric constant at the overlap between the gate and the source/drain extensions to complete formation of a transistor having low overlap capacitance.

FIGURE 6



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