

indication information, where the second time slot is after the first time slot.

[0059] In an implementation of the present disclosure, since the terminal needs to take a certain switch time to switch to the first communication state indicated by the PDCCH when the terminal receives the PDCCH, the terminal enters the first communication state indicated by the PDCCH in the second time slot after the terminal receives the PDCCH in the first time slot. The following will illustrate the technical solutions in the implementation of the present disclosure in combination with different application scenarios.

[0060] ➤ A first scenario is as follows.

[0061] The first communication state is the first cross-slot scheduling state. The terminal compares the first cross-slot scheduling state with a second cross-slot scheduling state that the terminal is currently in. When the first cross-slot scheduling state is different from the second cross-slot scheduling state, the terminal enters the first cross-slot scheduling state in the second time slot.

[0062] For example, the UE receives the PDCCH from the network device in a time slot n . The first cross-slot scheduling state is indicated by N bits in the PDCCH. For example, 2 bits in the PDCCH are indicative of the first cross-slot scheduling state. The UE compares the first cross-slot scheduling state indicated by the PDCCH with the second cross-slot scheduling state that the UE is currently in. If the first cross-slot scheduling state is different from the second cross-slot scheduling state, the UE enters the first cross-slot scheduling state in a time slot $n+x$. Herein, the second cross-slot scheduling state that the UE is currently in refers to a cross-slot scheduling state of the UE in the time slot n .

[0063] In an implementation of the present disclosure, there is an offset of x time slots between the second time slot and the first time slot, and x is a positive integer. Further, x is the maximum between a and S_c , a is a constant, and S_c is a slot offset corresponding to the second cross-slot scheduling state that the terminal is currently in.

[0064] For example, $x=\text{MAX}(a, S_c)$, where S_c is the slot offset corresponding to the second cross-slot scheduling state that the UE is currently in, and a is a constant (for example $a=1$). What needs to be illustrated is that the slot offset corresponding to the cross-slot scheduling state is $K0$ illustrated in FIG. 3, that is, an offset between a time slot where the data channel scheduled by the PDCCH locates and the time slot where the PDCCH locates.

[0065] In an implementation of the present disclosure, the first indication information includes N bits, where N is a positive integer. Different values of the first indication information are indicative of different first cross-slot scheduling states, and a correspondence between the first cross-slot scheduling states and the values of the N bits is configured by high-layer signaling. Herein, the high-layer signaling is radio resource control (RRC) signaling for example.

[0066] For example, $N=2$, that is, each first cross-slot scheduling state is indicated by 2 bits. “00” are indicative of a cross-slot scheduling state 1, and a slot offset corresponding to the cross-slot scheduling state 1 is 0, that is, scheduling is performed by crossing at least zero time slot, i.e., $S_c=0$ (in-slot scheduling is allowed). “01” are indicative of a cross-slot scheduling state 2, and a slot offset corresponding to the cross-slot scheduling state 2 is 1, that is, scheduling is performed by crossing at least one time slot, i.e., $S_c=1$. “10” are indicative of a cross-slot scheduling state 3, and a slot offset corresponding to the cross-slot scheduling state 3 is 2, that is, scheduling is performed by crossing at least two time slots, i.e., $S_c=2$. “11” are indicative of a cross-slot scheduling state 4, and a slot offset corresponding to the cross-slot scheduling state 4 is 3, that is, scheduling is performed by crossing at least three time slots, i.e., $S_c=3$. What needs to be illustrated is that the slot offset corresponding to the cross-slot scheduling state according to an implementation of the present disclosure refers to a minimum slot offset corresponding to the cross-slot scheduling state.

[0067] In an implementation of the present disclosure, the values of the N bits are determined by the number

PDCCH are indicative of the first MIMO transmission layer number state of the data channel (PDSCH or PUSCH), for example, 2 bits in the PDCCH are indicative of the first MIMO transmission layer number state. The UE compares the first MIMO transmission layer number state indicated by the PDCCH with the second MIMO transmission layer number state that the UE is currently in. If the first MIMO transmission layer number state is different from the second MIMO transmission layer number state, the UE enters the first MIMO transmission layer number state indicated by the PDCCH in the time slot $n+x$. Herein, the second MIMO transmission layer number state that the UE is currently in refers to the MIMO transmission layer number state that the UE is in in the time slot n .

[0093] In an implementation of the present disclosure, there is an offset of x time slots between the second time slot and the first time slot, and x is a positive integer.

[0094] For example, x is a constant. For example $x=1$. Alternatively, x is calculated based on a sub-carrier width of the current PDCCH and other information.

[0095] In the implementation of the present disclosure, the first indication information includes the N bits, where N is a positive integer, and different values of the first indication information are indicative of different first MIMO transmission layer number states. A correspondence between the first MIMO transmission layer number states and the values of the N bits is configured by the high-layer signaling. Herein, the high-layer signaling is the RRC signaling for example.

[0096] In an implementation of the present disclosure, a fault-tolerant mechanism is provided according to the implementation of the present disclosure. The fault-tolerant mechanism is as follows. When the terminal determines that the number (amount) of MIMO transmission layers for first data is larger than the number (amount) of transmission layers limited by the second MIMO transmission layer number state that the terminal is currently in, the terminal transmits a negative feedback message to the network device, where the first data refers to data indicated by the PDCCH that is received by the terminal in the first time slot.

[0097] For example, when the number of the second MIMO transmission layers for the data indicated by the PDCCH that is received by the UE in the time slot n exceeds the maximum number of transmission layers limited by the current state of the UE, the UE feeds back NACK to the network device.

[0098] Herein, the number of transmission layers limited by the second MIMO transmission layer number state that the terminal is currently in is defined as follows. For the PDSCH, the number of transmission layers limited by the second MIMO transmission layer number state that the terminal is currently in is the maximum number of transmission layers for a PDSCH expected to be received by the terminal. For the PUSCH, the number of transmission layers limited by the second MIMO transmission layer number state that the terminal is currently in is the maximum number of transmission layers for the PUSCH able to be transmitted by the terminal.

[0099] In an implementation of the present disclosure, when the number of transmission layers for data scheduled by the PDCCH is not identical to the number of transmission layers limited by the second MIMO transmission layer number state that the terminal is currently in, other domains in the PDCCH for example the first indication information and the power control information are still valid.

[0100] According to the technical solution of the implementation of the present disclosure, the network can be allowed to reasonably trigger the energy-saving function of the terminal. In the technical solution of the implementation of the present disclosure, the existing PDCCH is extended. The extended PDCCH supports both the scheduling function of the data channel and the energy-saving indication function of the terminal, and no additional energy-saving physical layer signal is required. In the implementation of the present disclosure, dynamic signaling such as the PDCCH is

adopted, and thus the terminal can enter the energy-saving state as soon as possible, and adaptive time of energy saving can be reduced from tens of microseconds to microsecond level. In addition, according to the technical solution of the implementations of the present disclosure, fault-tolerance processing in case of losing the PDCCH by the terminal is realized.

[0101] What needs to be noted is that the method adopted in the implementation of the present disclosure is based on the cross-slot scheduling state and the MIMO transmission layer number state. The important feature of the present disclosure is that the PDCCH is used to trigger switch between different communication states. The manner of switching the communication states can be extended to other signaling processes, and also can be extended to other energy-saving states of the terminal, such as a state of the maximum number of receiving antennas (i.e., maximum receiving antenna number state) of the terminal, a state of measurement periods (i.e., measure period state) of the terminal, etc..

[0102] FIG. 6 is a first schematic structural diagram illustrating a device for controlling communication states according to an implementation of the present disclosure. The device for controlling communication states is applied to a terminal. As illustrated in FIG. 6, the device for controlling communication states includes a receiving unit 601 and a controlling unit 602.

[0103] The receiving unit 601 is configured to receive a PDCCH from a network device in a first time slot, where the PDCCH carries first indication information indicative of a first communication state.

[0104] The controlling unit 602 is configured to enter the first communication state in a second time slot according to the first indication information, where the second time slot is after the first time slot.

[0105] In an implementation, the first communication state is a first cross-slot scheduling state. The controlling unit 602 is configured to compare the first cross-slot scheduling state with a second cross-slot scheduling state that the terminal is currently in, and enter the first cross-slot scheduling state in the second time slot when the first cross-slot scheduling state is different from the second cross-slot scheduling state.

[0106] In an implementation, an offset of x time slots exists between the second time slot and the first time slot, where x is a positive integer.

[0107] In an implementation, x is the maximum between a and S_c , a is a constant, and S_c is a slot offset corresponding to the second cross-slot scheduling state that the terminal is currently in.

[0108] In an implementation, the first indication information includes N bits, where N is a positive integer, different values of the first indication information are indicative of different first cross-slot scheduling states, and a correspondence between the first cross-slot scheduling states and the values of the N bits is configured by high-layer signaling.

[0109] In an implementation, the values of the N bits are determined by the number of cross-slot scheduling states of a PUSCH and the number of cross-slot scheduling states of a PDSCH that are configured by the high-layer signaling.

[0110] In an implementation, when the number of the cross-slot scheduling states of the PUSCH and the number of the cross-slot scheduling states of the PDSCH are not configured by the high-layer signaling, the values of the N bits are 0. When the number of the cross-slot scheduling states of the PUSCH and/or the number of the cross-slot scheduling states of the PDSCH are configured by the high-layer signaling, the values of the N bits are 1.

[0111] In an implementation, each of the first cross-slot scheduling states corresponds to a set of slot offsets, where the set of slot offsets include a first slot offset for the PDSCH and a second slot offset for the PUSCH.

[0112] In an implementation, each of the first cross-slot scheduling states corresponds to a slot offset, where the slot offset is a first slot offset for the PDSCH or a second slot offset for the PUSCH.

different values of the first indication information are indicative of different first MIMO transmission layer number states, and a correspondence between the first MIMO transmission layer number states and the values of the N bits is configured by high-layer signaling.

[0124] In an implementation, the device further includes the transmitting unit 603 configured to transmit a negative feedback message to the network device, when the terminal determines that the number of MIMO transmission layers for first data is larger than the number of transmission layers limited by the second MIMO transmission layer number state that the terminal is currently in, where the first data is data indicated by the PDCCH that is received by the terminal in the first time slot.

[0125] In an implementation, the number of transmission layers limited by the second MIMO transmission layer number state that the terminal is currently in is the maximum number of transmission layers for a PDSCH expected to be received by the terminal. Alternatively, the number of transmission layers limited by the second MIMO transmission layer number state that the terminal is currently in is the maximum number of transmission layers for the PUSCH able to be transmitted by the terminal.

[0126] A person of ordinary skill in the art shall understand that in the implementations of the present disclosure, for related description of the above device for controlling communication states, reference can be made to the related description of the method for controlling communication states according to the implementation of the implementation of the present disclosure.

[0127] FIG. 7 is a second schematic structural diagram illustrating a device for controlling communication states according to an implementation of the present disclosure. The device for controlling communication states is applied to a network device. As illustrated in FIG. 7, the device for controlling communication states includes a transmitting unit 701.

[0128] The transmitting unit 701 is configured to transmit a PDCCH to a terminal, where the PDCCH carries first indication information indicative of a first communication state. The first indication information is used for directing the terminal to enter the first communication state in a second time slot when the first indication information is received by the terminal in a first time slot, and the second time slot is after the first time slot.

[0129] In an implementation, the first communication state is a first cross-slot scheduling state.

[0130] In an implementation, an offset of x time slots exists between the second time slot and the first time slot, where x is a positive integer.

[0131] In an implementation, x is the maximum between a and S_c , a is a constant, and S_c is a slot offset corresponding to a second cross-slot scheduling state that the terminal is currently in.

[0132] In an implementation, the first indication information includes N bits, where N is a positive integer, different values of the first indication information are indicative of different first cross-slot scheduling states, and a correspondence between the first cross-slot scheduling states and the values of the N bits is configured by high-layer signaling.

[0133] In an implementation, each of the first cross-slot scheduling states corresponds to a set of slot offsets, where the set of slot offsets include a first slot offset for a PDSCH and a second slot offset for a PUSCH.

[0134] In an implementation, each of the first cross-slot scheduling states corresponds to a slot offset, where the slot offset is the first slot offset for the PDSCH or the second slot offset for the PUSCH.

[0135] In an implementation, the first slot offset for the PDSCH is different from the second slot offset for the PUSCH.

[0136] In an implementation, the first communication state is a first MIMO transmission layer number state of a data channel.

[0137] In an implementation, the offset of x time slots exists between the second time slot and the first time slot, where x is a positive integer.

[0138] In an implementation, the first indication information includes the N bits, where N is a positive integer, different values of the first indication information are indicative of different first MIMO transmission layer number states, and a correspondence between the first MIMO transmission layer number states and the values of the N bits is configured by the high-layer signaling.

[0139] In an implementation, the PDCCH further carries at least one of: frequency-domain scheduling information of the data channel, time-domain scheduling information of the data channel, MCS indication information, power control information, CSI trigger information, and BWP switch indication information.

[0140] A person of ordinary skill in the art shall understand that in an implementation of the present disclosure, for related description of the above device for controlling communication states, reference can be made to the related description of the method for controlling communication states according to the implementation of the present disclosure.

[0141] FIG. 8 is a schematic structural view illustrating a communication device 800 according to an implementation of the present disclosure. The communication device 800 may be a terminal or a network device. The communication device 800 illustrated in FIG. 8 includes a processor 810. The processor 810 can invoke and run at least one computer program in a memory to implement the method in the implementation of the present disclosure.

[0142] In an implementation, as illustrated in FIG. 8, the communication device 800 further includes a memory 820. The processor 810 can invoke and run the computer program in the memory 820 to implement the method in the implementation of the present disclosure.

[0143] The memory 820 may be a single device independent of the processor 810, and may also be integrated in the processor 810.

[0144] In an implementation, as illustrated in FIG. 8, the communication device 800 may further include a transceiver 830. The processor 810 can control the transceiver 830 to communication with other devices, for example, to transmit information or data to the other devices or receive information or data from the other devices.

[0145] In an implementation, the transceiver 830 may include a transmitter and a receiver. The transceiver 830 may further include one or more antennas.

[0146] The communication device 800 may be the network device in the implementations of the present disclosure, and the communication device 800 can implement corresponding procedures realized by the network device in the methods in the implementations of the present disclosure, which will not be repeated herein for simplicity.

[0147] The communication device 800 may be the mobile terminal/terminal in the implementations of the present disclosure, and the communication device 800 can implement corresponding procedures realized by the mobile terminal/terminal in the implementations of the present disclosure, which will not be repeated herein for simplicity.

[0148] FIG. 9 is a schematic structural diagram illustrating a chip according to an implementation of the present disclosure. The chip 900 illustrated in FIG. 9 includes a processor 910. The processor 910 can invoke and run at least one computer program stored in a memory to implement the methods in the implementation of the present disclosure.

[0149] In an implementation, as illustrated in FIG. 9, the chip 900 further includes a memory 920. The processor