CLAIMS

1. A package for an electric device, comprising:

a substrate comprising at least a piezoelectric layer;

operational device structures on a first surface of the piezoelectric layer;

an integrally formed package layer structure on the first surface comprising at least a mechanical support layer covering the first surface of the substrate and enclosing the operational device structures in a cavity;

a first contact pad on the first surface of the substrate electrically connected to the operational device structures;

a second contact pad on a second surface opposite to the first surface;

a via through the substrate and electrically interconnecting the first contact pad and the second contact pad; and

a barrier layer over at least the mechanical support layer and having an opening for coupling the first contact pad to another substrate.

2. The package of claim 1, wherein:

the mechanical support layer comprises a silicon oxide layer that forms domes enclosing the operational device structures;

a protection layer covers the mechanical support layer;

the barrier layer covers the protection layer; and

the first contact pad is exposed on the first surface.

3. The package of claim 1, wherein the first contact pad is covered by the package layer structure, and wherein an external contact of the operational device structures is provided solely by the second contact pad.

4. The package of claim 1, wherein:

the package is connected to the other substrate by connecting the first contact pad with a third contact pad of the other substrate by bonding via a solder bump, a pillar, or a stud bump through the opening of the barrier layer.

5. The package of claim 1, wherein the operational device structures are part of a surface acoustic wave (SAW) device or a bulk acoustic wave (BAW) device.

6. The package of claim 1, wherein the substrate is a wafer comprising the electric device.

7. A method of manufacturing a package, comprising:

forming device structures for electric devices on a first surface of a first wafer and forming first pads connected to the device structures, the first wafer comprising a piezoelectric layer;

applying, over the device structures, an integrated package layer structure that seals to the first surface and forms a cavity between the integrated package layer structure and the first surface of the first wafer to enclose device structures within the cavity, wherein the integrated package layer includes a mechanical support layer;

reducing a thickness of the first wafer from a second surface opposite to the first surface; forming holes in the second surface to a depth until bottom parts of the first pads are exposed;

depositing a metallization on the second surface electrically contacting the first pads in the holes; and

forming second pads on the second surface, wherein applying the integrated package layer structure includes forming a barrier layer over at least the mechanical support layer and having an opening for coupling the first pads to another substrate.

8. The method of claim 7, wherein forming the holes comprises ablation of material from the first wafer by drilling, etching or by using a laser beam.

9. The method of claim 7, further comprising:

arranging the first wafer and a second wafer in a stack, wherein the second surface of the first wafer is facing a surface of the second wafer; and

directly connecting the second pads of the first wafer with pads of the second wafer.

10. The method of claim 7, further comprising:

exposing pads of a second wafer; and

arranging the first wafer and the second wafer in a stack, wherein the second surface of the first wafer faces a surface of the second wafer; and

directly connecting the second pads of the first wafer and the pads of the second wafer.

11. The method of claim 7, further comprising:

forming trenches in the first surface of the first wafer and a surface of a second wafer;

bonding the first surface of the first wafer to a temporary carrier, wherein reducing the thickness of the first wafer from the second surface exposes the trenches;

forming the second pads on the second surface on or from the metallization;

exposing the first pads of the second wafer;

arranging the first wafer and second wafer in a stack where the second surface of the first wafer faces the first surface of the second wafer and directly connecting the second pads of the first wafer and the first pads of the second wafer; and

reducing the thickness of the second wafer from the second surface to expose the trenches in the second wafer.

12. The method of claim 7, wherein the first wafer comprises a thin piezoelectric layer on a carrier substrate, wherein the method further comprises:

forming trenches that cut only through the piezoelectric layer after applying the integrated package layer structure.

13. The method of claim 7, wherein applying the integrated package layer structure comprises forming the barrier layer as a topmost layer of the integrated package layer structure, and wherein the barrier layer is a metal layer, a SiN layer, or any other layer that can function as a barrier against humidity.

14. The method of claim 7, wherein depositing the metallization and forming the second pads comprise forming a redistribution layer in or on the metallization and forming the second pads that are laterally shifted relative to the first pads, and wherein a conductor line of the redistribution layer electrically connects the second pads to the metallization in the holes.

15. The method of claim 7, further comprising preparing a second wafer and bonding the second wafer on the second pads.

16. The method of claim 11, wherein the temporary carrier comprises a same material as the first wafer, and wherein the temporary carrier is separated from the first wafer after reducing the thickness of the second wafer.