CLAIMS

I/We claim:

1. A wafer testing system, comprising:

an interposer having a first surface and a second surface facing away from the first surface, wherein at least one contact pad at the first surface is electrically connected with at least one contact pad at the second surface;

a wafer translator having:

a substrate having a first side facing the interposer and a second side facing away from the first side, the second side positioned to face toward a wafer,

a first terminal at the first side,

a second terminal at the second side, positioned to contact a corresponding wafer terminal, wherein the first terminal is larger than the second terminal, and

an electrical pathway connecting the first and second terminals; and

a translator support configured to receive the wafer translator, the translator support having a seal configured to seal a space between the wafer translator and the interposer.

2. The wafer testing system of claim 1 wherein the translator support includes a pathway configured to fluidly connect the space between the wafer translator and the interposer with a first vacuum.

3. The wafer testing system of claim 1 wherein:

the translator support includes a ring having a groove configured to receive the seal; and

the seal includes a generally flexible material at least partially received in the groove of the ring.

4. The wafer testing system of claim 1 wherein:

the translator support includes a ring having a groove; and

the seal includes a base portion and an upper portion extending from the base portion, the base portion being received in the groove of the ring.

5. The wafer testing system of claim 1 wherein:

the translator support includes a ring having a groove with a flange;

the seal includes a base portion and an upper portion extending from the base portion; and

the base portion is received in the groove of the ring and retained by the flange of the groove.

6. The wafer testing system of claim 1 wherein:

the translator support includes a ring having a groove with a flange;

the seal includes a base portion and an upper portion extending from the base portion;

the base portion is received in the groove of the ring and retained by the flange of the groove; and

the upper portion is angled circumferentially outward with respect to the translator support.

7. A method for establishing contact with a wafer having a bond pad, comprising:

placing an interposer to face a wafer translator,

placing the wafer translator to face toward the wafer, the wafer translator having a terminal facing the bond pad of the wafer;

sealing a first space between the interposer and the wafer translator using a first seal; and

drawing a first vacuum on the first space to

contact the bond pad of the wafer with the terminal of the wafer translator.

8. The method of claim 18, further comprising adjusting at least one of the first and second vacuums based on a target contact force between the terminal and the bond pad.

9. The method of claim 18, further comprising adjusting at least one of the first and second vacuums such that the terminal and the bond pad are in electrical and mechanical contact.

10. The method of claim 18, further comprising:

placing the wafer on a chuck, the wafer having a first side facing the wafer translator and a second side facing the chuck;

establishing a third vacuum between the second side of the wafer and the chuck; and

adjusting at least one of the first, second, and third vacuums based on a target contact force between the terminal and the bond pad.

11. The method of claim 18 wherein:

the bond pad is a first bond pad;

the terminal is a first terminal;

the wafer further includes a plurality of additional bond pads;

the wafer translator further includes a plurality of additional terminals corresponding to the bond pads of the wafer; and

the method further includes adjusting at least one of the first and second vacuums based on a target contact force between the plurality of terminals and the corresponding bond pads.

12. The method of claim 18, further comprising controlling forces on the wafer translator by adjusting the first vacuum in the first space and the second vacuum in the second space to be different.

13. The wafer testing system of claim 1 wherein the seal is a first seal, the wafer testing system further comprising:

a second seal configured to seal a space between the wafer and the wafer translator.

14. The wafer testing system of claim 1, further comprising:

a device interface board having a first surface and a second surface facing away from the first surface, the second surface of the device interface board facing the interposer, wherein the device interface board has electrical interconnections between the first and second surfaces.

15. The wafer testing system of claim 13 wherein the first seal seals the space between the wafer translator and the interposer under a first vacuum, and the second seal seals the space between the wafer translator and the wafer under a second vacuum.

16. The wafer testing system of claim 15 wherein the first and second vacuums are individually operable.

17. The wafer testing system of claim 15, further comprising a source of a third vacuum in a fluid communication with the space between the wafer and a prober, wherein the first, second and third vacuums are individually operable.

18. The method of claim 7, further comprising:

sealing a second space between the wafer and the wafer translator using a second seal;

establishing a second vacuum in the second space; and

contacting the bond pad of the wafer with the terminal of the wafer translator under the first and second vacuums.

CLAIMS

1. A wafer testing system, comprising:

an interposer having a first surface and a second surface facing away from the first surface, wherein at least one contact pad at the first surface is electrically connected with at least one contact pad at the second surface;

a wafer translator having:

a substrate having a first side facing the interposer and a second side facing away from the first side, the second side positioned to face toward a wafer,

a first terminal at the first side,

a second terminal at the second side, positioned to contact a corresponding wafer terminal, wherein the first terminal is larger than the second terminal, and

an electrical pathway connecting the first and second terminals; and

a translator support configured to receive the wafer translator, the translator support having a seal configured to seal a space between the wafer translator and the interposer.

2. The wafer testing system of claim 1 wherein the translator support includes a pathway configured to fluidly connect the space between the wafer translator and the interposer with a first vacuum source.

3. The wafer testing system of claim 1 wherein:

the translator support includes a ring having a groove configured to receive the seal; and

the seal includes a generally flexible material at least partially received in the groove of the ring.

4. The wafer testing system of claim 1 wherein:

the translator support includes a ring having a groove; and

the seal includes a base portion and an upper portion extending from the base portion, the base portion being received in the groove of the ring.

5. The wafer testing system of claim 1 wherein:

the translator support includes a ring having a groove with a flange;

the seal includes a base portion and an upper portion extending from the base portion; and

the base portion is received in the groove of the ring and retained by the flange of the groove.

6. The wafer testing system of claim 1 wherein:

the translator support includes a ring having a groove with a flange;

the seal includes a base portion and an upper portion extending from the base portion;

the base portion is received in the groove of the ring and retained by the flange of the groove; and

the upper portion is angled circumferentially outward with respect to the translator support.

7. A method for establishing contact with a wafer having a bond pad, comprising:

placing an interposer to face a wafer translator,

placing the wafer translator to face toward the wafer, the wafer translator having:

a first side facing the interposer and a second side facing the wafer, and

a first terminal at the first side and a second terminal at the second side, wherein the second terminal faces the bond pad of the wafer, and wherein the first terminal is larger than the second terminal;

sealing a first space between the interposer and the wafer translator using a first seal; and

drawing a first vacuum on the first space to contact the bond pad of the wafer with the second terminal of the wafer translator.

8. The method of claim 7, further comprising:

sealing a second space between the wafer and the wafer translator using a second seal;

establishing a second vacuum in the second space; and

contacting the bond pad of the wafer with the second terminal of the wafer translator under the first and second vacuums.

9. The method of claim 8, further comprising adjusting at least one of the first and second vacuums based on a target contact force between the second terminal and the bond pad.

10. The method of claim 8, further comprising adjusting at least one of the first and second vacuums such that the second terminal and the bond pad are in electrical and mechanical contact.

11. The method of claim 8, further comprising:

placing the wafer on a chuck, the wafer having a first side facing the wafer translator and a second side facing the chuck;

establishing a third vacuum between the second side of the wafer and the chuck; and

adjusting at least one of the first, second, and third vacuums based on a target contact force between the second terminal and the bond pad.

12. The method of claim 8 wherein:

the bond pad is a first bond pad;

the terminal is a first terminal;

the wafer further includes a plurality of additional bond pads;

the wafer translator further includes a plurality of additional terminals corresponding to the bond pads of the wafer; and

the method further includes adjusting at least one of the first and second vacuums based on a target contact force between the plurality of additional terminals and the corresponding bond pads of the wafer.

13. The method of claim 8, further comprising controlling forces on the wafer translator by adjusting the first vacuum in the first space and the second vacuum in the second space to be different.

14. The wafer testing system of claim 1 wherein the seal is a first seal, the wafer testing system further comprising:

a second seal configured to seal a space between the wafer and the wafer translator.

15. The wafer testing system of claim 1, further comprising:

a device interface board having a first surface and a second surface facing away from the first surface, the second surface of the device interface board facing the interposer, wherein the device interface board has electrical interconnections between the first and second surfaces.

16. The wafer testing system of claim 14 wherein the first seal seals the space between the wafer translator and the interposer under a first vacuum, and the second seal seals the space between the wafer translator and the wafer under a second vacuum.

17. The wafer testing system of claim 16 wherein the first and second vacuums are individually operable.

18. The wafer testing system of claim 16, further comprising a third vacuum in a fluid communication with the space between the wafer and a prober, wherein the first, second and third vacuums are individually controllable.