SEMICONDUCTOR DIES WITH RECESSES, ASSOCIATED LEADFRAMES, AND ASSOCIATED SYSTEMS AND METHODS

TECHNICAL FIELD

[0001] The present disclosure is directed generally to semiconductor dies with recesses, associated leadframes, and associated systems and methods.

BACKGROUND

[0002] Semiconductor processing and packaging techniques are continually evolving to meet industry demands for devices with improved performance and reduced size and cost. Electronic products require packaged semiconductor assemblies with a high density of devices in a relatively small space. For example, the space available for memory devices, processors, displays and other semiconductor devices is continually decreasing in cell phones, personal digital assistants, laptop computers and many other products. Accordingly, a need exists to increase the density of semiconductor devices and components within the confined footprint of a semiconductor assembly. One technique for increasing the density of semiconductor devices within a given footprint is to stack semiconductor dies. A challenge with this technique, however, is providing adequate electrical interconnects within and between the stacked dies.

[0003] One approach to addressing the challenges associated with stacked semiconductor dies is to use a leadframe having a support paddle that supports the lowest die, and leadfingers that provide electrical connections between the stack of dies and devices external to the finished package. While this arrangement has proven to be suitable for many purposes, the continual pressure to reduce not only the footprint of the package but also the overall volume of the package has created the need for still smaller and more efficiently packaged dies.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] Figure 1 is a partially schematic, cross-sectional side elevation view of a portion of a package configured in accordance with an embodiment of the disclosure.

[0005] Figure 2 is a partially schematic, exploded plan view illustration of package components, including a semiconductor die and a leadframe having leadfingers and a support paddle configured in accordance with an embodiment of the disclosure.

[0006] Figure 3 is a partially schematic, exploded plan view illustration of a semiconductor die and a leadframe having a support paddle configured in accordance with an embodiment of the disclosure.

[0007] Figure 4 is a partially schematic, exploded plan view illustration of a semiconductor die and a leadframe having a support paddle configured in accordance with an embodiment of the disclosure.

[0008] Figure 5 is a flow diagram illustrating methods for packaging semiconductor dies in accordance with several embodiments of the disclosure.

[0009] Figure 6 is a partially schematic, block diagram illustrating a system in which packages may be incorporated in accordance with still further embodiments of the disclosure.

DETAILED DESCRIPTION

[0010] Several embodiments of the present disclosure are described below with reference to packaged semiconductor devices and assemblies, and methods for forming packaged semiconductor devices and assemblies. Many details of certain embodiments are described below with reference to semiconductor dies. The term "semiconductor die" is used throughout to include a variety of articles of manufacture, including for example, individual integrated circuit dies and/or dies having other semiconductor features. Many specific details of certain embodiments are set forth in Figures 1-6 and the following text to provide a thorough understanding of these embodiments. Several other embodiments can have different configurations, components and/or processes than those described in this section. A person skilled in the relevant art, therefore, will appreciate that

additional embodiments may be practiced without several details of the embodiments shown in Figures 1-6.

[0011] Figure 1 is a partially schematic, cross-sectional view of a system 100 that includes a package 101 (a portion of which is shown) configured in accordance with a particular embodiment. The package 101 can include a leadframe 130 having a support paddle 131 carrying one or more semiconductor dies 110. For purposes of illustration, the leadframe 130 is shown carrying four stacked semiconductor dies 110, shown as first, second, third and fourth semiconductor dies 110a, 110b, 110c, and 110d, respectively. In other embodiments, the leadframe 130 can carry more or fewer dies 110, for example, a single die 110 or two stacked dies 110. In any of these embodiments, the die(s) 110 can include one or more recesses 114 that receive the support paddle 131, as described in further detail below.

[0012] In an embodiment shown in Figure 1, each of the dies 110 has a first (e.g., downwardly facing) die surface 111, and a second (e.g., upwardly facing) second die surface 112. The illustrated first die surface 111 includes two recesses 114, one along each of two opposing edges of the first die surface 111, and one of which is visible in Figure 1. The recesses 114 can locally reduce a thickness T of the die 110. Suitable techniques for cutting the recesses 114 in the dies 110 are included in U.S. Patent No. 7,218,001, assigned to the assignee of the present application and incorporated herein by reference. In the arrangement shown in Figure 1, at least part of the support paddle 131 is received in the recess 114 of the first die 110a. In a particular embodiment, the recess 114 is deep enough so that a first paddle surface 133 (e.g., an outwardly facing surface) is flush with or recessed from the first die surface 111. Accordingly, the addition of the support paddle 131 beneath the first die 110a does not add to the overall thickness T of the first die 110a alone. The support paddle 131 can further include a second paddle surface 134 that faces into the recess 114 and away from the first paddle surface 133. A paddle adhesive 135 can adhesively bond the support paddle 131 to surfaces 115 of the recess 114.

[0013] In a particular embodiment, the overall thickness of the first die 110a can be about 120 microns, and the recess 114 can have a depth of about 60 microns. The combined thickness of the support paddle 131 and the paddle adhesive 135 can be about 60 microns or less, so that the first paddle surface 133 is flush with or recessed from the adjacent first die surface 111. In other

embodiments, the foregoing features can have different dimensions, while the support paddle 131 still does not add to the overall thickness T of the die 110a and the support paddle 131 combined. In still further embodiments, the support paddle 131 can be only partially received in the recess 114, so that it protrudes, in part, from the recess 114. In such instances, the support paddle 131 does add to the overall thickness of the die 110a and the support paddle 131 combined, but not as much as if the recess 114 were not present.

[0014] When the package 101 includes multiple dies 110, the additional dies can be stacked on the first die 110a and attached with corresponding layers of die adhesive 116. The layers of die adhesive 116 can be relatively thin to reduce the overall package thickness and/or the likelihood for thermal conductivity mismatches resulting from differing coefficients of thermal expansion. Each of the dies 110 can include a bond site 113 located proximate to and accessible from the second die surface 112. The bond sites 113 and the recesses 114 of the stacked dies 110 can be arranged so that the recesses 114 of an upper die (e.g., the second die 110b) lie directly over corresponding bond sites 113 of the next lower die (e.g., the first die 110a) in the stack. Accordingly, the recesses 114 of the upper dies can house, accommodate and/or receive electrical connections between the leadframe 130 and the bond sites 113 of the lower die.

[0015] To support electrical connections to the semiconductor dies 110, the leadframe 130 includes leadfingers 132 that extend inwardly toward the dies 110. Individual leadfingers 132 can be connected to corresponding bond sites 113 of the dies 110 with wire bonds 103. When the package 101 includes multiple dies 110, an individual leadfinger 132 may be connected to corresponding bond sites 113 of each of the dies 110. The recesses 114 can reduce or eliminate the likelihood for the wire bonds 103 to contact the semiconductor die 110 in which the recesses 114 are formed.

[0016] Multiple leadfingers 132 may be arranged side by side in a direction extending transverse to the plane of Figure 1, and may accordingly form a leadfinger plane L, an edge of which is visible in Figure 1. The support paddle or paddles 131 may extend in a direction generally transverse to the plane of Figure 1 and may accordingly form a paddle plane P. In a particular embodiment, the leadfinger plane L is offset from the paddle plane P in a direction generally aligned with the thickness dimension T of the dies 110. This arrangement can reduce the length of the wire

bond 103 required to connect the leadfinger 132 to the furthest die (e.g., the fourth die 110d). In other embodiments, the leadfinger plane L and the paddle plane P can have arrangements other than that shown in Figure 1. For example, when the package 101 includes only the first die 110a, the leadfinger plane L may be coplanar with the paddle plane P. In any of these arrangements, once the electrical connections between the leadframe 130 and the die(s) 110 are formed, the die(s) 110, the wire bonds 103, the support paddle 131, and the leadfingers 132 can be at least partially encapsulated with an encapsulant 102. Portions of the leadfingers 132 that project outwardly from the encapsulant 102 can then be trimmed, shaped, and/or otherwise formed to provide connections to external components.

[0017] Figure 2 is a partially exploded, schematic plan view illustration of components of an embodiment of the package 101, including the leadframe 130 and the first die 110a shown in Figure 1. The leadframe 130 can be formed from a unitary thin sheet of conductive material (e.g., gold), using a stamping process or another suitable process. The leadframe 130 includes a frame member 136, which temporarily carries the inwardly extending leadfingers 132 and the support paddle 131. The support paddle 131 is positioned inwardly from the leadfingers 132 and is supported relative to the frame member 136 by removable ties 137. In this particular embodiment, the support paddle 131 includes a paddle surface 138 that is divided over a first portion 139a and second portion 139b. Accordingly, the paddle surface 138 is discontinuous in this embodiment. When the first semiconductor die 110a is inverted and positioned face down on top of the frame member 136 (as indicated by arrow A), each of the recesses 114 is aligned with and receives a corresponding one of the first and second portions 139a, 139b. The bond sites 113 (Figure 1) on the second die surface 112 are then electrically connected to the leadfingers 132 at corresponding leadfinger bond sites 141 e.g., using standard wire bonds, or other suitable conductive couplers. If further dies are to be stacked on the first die 110a, each one is stacked and connected to the leadfingers 132 before the next die is stacked and electrically connected to the leadframe 130. After all the dies have been stacked and electrically connected to the leadframe 130, the assembly is placed in a mold and encapsulated, after which the frame member 136, the ties 137 and (optionally) portions of the leadfingers 132 are removed.

[0018] In a particular embodiment of the arrangement shown in Figure 2, the leadframe 130 includes an opening 140 between the first and second portions 139a, 139b. The first and second portions 139a, 139b can be elongated so as to fit into the corresponding elongated recesses 114 of the first semiconductor die 110a. Because the first die 110a is rectangular and the recesses 114 are aligned with opposing edges of the first semiconductor die 110a, the first and second portions 139a, 139b of the support paddle 131 can also be aligned generally parallel to each other. In other embodiments, the leadframe 130 can have other arrangements that also support one or more semiconductor dies 110. Representative arrangements are described below with reference to Figures 3 and 4.

[0019] Beginning with Figure 3, a leadframe 330 in accordance with another embodiment includes a frame member 136 and leadfingers 132 arranged generally similarly to the corresponding components described above with reference to Figure 2. The leadframe 330 further includes a support paddle 331 having four spaced apart portions 339 (shown as first, second, third and fourth portions 339a, 339b, 339c, and 339d, respectively) positioned around a central opening 340. Each of the portions 339a can be connected to the frame member 136 with a corresponding tie 337. The first semiconductor die 110a can include elongated recesses 114 (shown in dashed lines) generally similar to those shown in Figure 2 so as to accommodate and receive the portions 339a-339d of the support paddle 331. In another embodiment, the first semiconductor die 110a can instead include four separate recesses 314a-314d, each positioned at a corner of the first die 110a to receive a corresponding one of the support paddle portions 339a-339d. The support paddle portions 339a-339d can be arranged symmetrically, e.g., so that a diagonal line connecting the first and third portions 339a, 339c bisects a diagonal line connecting the second and fourth portions 339b, 339d. In other embodiments, the paddle portions 339 can have other symmetric or asymmetric arrangements.

[0020] Figure 4 illustrates a leadframe 430 that carries a corresponding semiconductor die 410 in accordance with another embodiment. The leadframe 430 can include a frame member 436 that carries inwardly extending leadfingers 432 and a unitary support paddle 431. The support paddle 431 can have a central opening 440, and can be temporarily supported relative to the frame member 436 with ties 437. Accordingly, the support paddle 431 can have a shape generally similar to a

picture frame, and in a particular embodiment, can have four portions 439a-439d that are integrally connected to form a unitary structure. The corresponding semiconductor die 410 includes a corresponding recess 414 positioned around its periphery to mirror the arrangement of the support paddle 431. Accordingly, when the semiconductor die 410 is inverted and placed on the leadframe 430, the generally frame-shaped support paddle 431 is received in the generally framed-shaped recess 414 of the semiconductor die 410, and the central portion of the semiconductor die 410 is received in the central opening 440 of the leadframe 430.

[0021] Figure 5 is a flow diagram of a process 500 for forming packaged semiconductor devices in accordance with several embodiments. For purposes of illustration, features of several embodiments are shown together in Figure 5. It will be understood by one of ordinary skill in the relevant art that further particular embodiments may be practiced with fewer than all the steps identified in Figure 5, and that in other embodiments, additional steps may be performed in addition to those identified in Figure 5.

[0022] Process portion 501 includes positioning a semiconductor die and a leadframe proximate to each other. In process portion 502, a support paddle is received in a recess of the semiconductor die. For example, a support paddle or support paddle portion having any of the configurations described above with reference to Figures 1-4 be can be received in one or more corresponding recesses of a semiconductor die.

[0023] Process portion 503 includes positioning a support paddle (having a paddle surface with an opening extending through it) relative to the semiconductor die. Process portion 503 can be performed in addition to or in lieu of process portion 502. For example, in the context of the arrangements describe above with reference to Figures 1-4, the opening in the support paddle can allow the support paddle to be positioned so that the paddle surface is received or partially received in one or more recesses of the die. However, in other embodiments, a paddle having an opening extending through it can support a semiconductor die without necessarily having the support surfaces received in a recess of the die.

[0024] In any of the foregoing embodiments, the support paddle can be attached to the die (process portion 504), and the die can be electrically connected to leadfingers (process portion 505). In process portion 506, the die, the leadfingers, and/or the support paddle can be encapsulated to

protect these components. In process portion 507, a frame member, which may temporarily support the leadfingers and the support paddle relative to the die, can be removed, typically after the encapsulation process has been completed.

[0025] One feature of semiconductor packages configured and/or manufactured in accordance with at least some of the foregoing embodiments described above with reference to Figures 1-5 is that they include support paddles received in one or more recesses of a corresponding semiconductor die. This arrangement can reduce the overall thickness of the semiconductor package because the thickness of the support paddle is not cumulative to the thickness of the semiconductor die. Instead, the support paddle can be fully or partially recessed into the adjacent surface of the die. The presence of the recesses in the die can allow the overall thickness of the die to remain relatively high (e.g., above 100 microns) without adding to the overall thickness of the combined die/support paddle. Dies having a thickness in the foregoing range can have good refresh margins and/or read/write speeds, without compromising on the compact (e.g., thin) profile of the packaged dies. In further particular embodiments, the support paddles can form part of an overall leadframe that also includes leadfingers for electrical connections to the semiconductor die. Accordingly, the leadframe can provide both the low-profile support described above, and electrical connections with external devices.

[0026] Another feature of at least some of the foregoing embodiments is that the support paddle can include multiple paddle surfaces separated by an opening. As a result, the amount of material required to form the support paddle can be reduced when compared to a conventional paddle that has a solid geometry generally mirroring the footprint of the die that it supports. Reducing the amount of material for the support paddle can reduce the cost of the paddle and therefore the cost of the completed package. Despite the reduction in the size of the support paddle 131, the combination of the support paddle 131, the ties 137 and the leadframe 130 provide adequate support to the semiconductor die or dies they carry during the wire bond and encapsulation steps

[0027] Any of the semiconductor packages described above with reference to Figures 1-5 can be incorporated into any of a myriad of larger and/or more complex systems, a representative example of which is a system 600 shown schematically in Figure 6. The system 600 can include a

processor 602, a memory 604 (e.g., SRAM, DRAM, flash memory and/or other memory device), input/output devices 606 and/or other subsystems or components 608. Semiconductor packages having any one or a combination of the features described above with reference to Figures 1-5 may be included in any of the components shown in Figure 6. The resulting system 600 can perform any of a wide variety of computing, processing, storage, sensing, imaging and/or other functions. Accordingly, the representative system 600 includes, without limitation, computers and/or other data processors, for example, desktop computers, laptop computers, Internet appliances, hand-held devices (e.g., palm-top computers, wearable computers, cellular or mobile phones, personal digital assistants, music players, etc.), multi-processor systems, processor-based or programmable consumer electronics, network computers and mini computers. Other representative systems 600 may be housed in a single unit or distributed over multiple interconnected units (e.g., through a communication network). The components of the system 600 can accordingly include local and/or remote memory storage devices, and any of a wide variety of computer readable media.

[0028] From the foregoing, it will be appreciated that specific embodiments have been described herein for purpose of illustration, but that the foregoing systems and methods may have other embodiments as well. For example, while the leadfingers and support paddles were described above in the context of a generally uniform and continuous leadframe, and accordingly have similar or identical material properties, in other embodiments, the leadfingers and the paddle supports can have different compositions, and/or non-unitary arrangements. The support paddles can have shapes and/or arrangements other than those specifically described above, for example, opposing "C" shaped support portions, more than four support portions, and/or others. The support paddle can be secured to the die with arrangements other than those shown in the Figures, e.g., a thin film that extends over both the support paddle and the adjacent (flush or semi-flush) die surface.

[0029] Certain features described in the context of particular embodiments may be combined or eliminated in other embodiments. For example, several of the embodiments described above were described in the context of paddle supports received in recesses of corresponding semiconductor dies, but in other embodiments, the paddle supports can include multiple spaced apart portions, or openings between paddle support portions, without necessarily being received in recesses of corresponding semiconductor dies. In another example, the semiconductor die shown in

Figure 4 can be used with the support paddles shown in Figures 1-3. Further, while certain advantages may be associated with certain embodiments, other embodiments may also exhibit such advantages, and not all embodiments need necessarily exhibit such advantages. Accordingly, the disclosure can include other embodiments not shown or described above.

CLAIMS

I/We claim:

1. A semiconductor system, comprising:

a first semiconductor die having a first surface and a second surface facing opposite from the first surface, the first surface having a first die recess, and the second surface having a bond site;

a second semiconductor die stacked relative to the first semiconductor die, the second semiconductor die having a third surface facing the second surface of the first semiconductor die, the third surface having a second die recess;

a lead finger extending toward the first semiconductor die, the lead finger having a contact terminal;

a wirebond extending between the contact terminal of the lead finger and the bond site of the first semiconductor die;

a support paddle carrying the first semiconductor die, the support paddle having a first paddle surface at least partially received in the first die recess and a second paddle surface opposite the first paddle surface; and

an adhesive directly between the second surface of the first semiconductor die and the third surface of the second semiconductor die, wherein a portion of the wirebond is encapsulated by the adhesive in a space between the second die recess and the second surface of the first semiconductor die.

2. The system of claim 1 wherein:

the first die recess is one of two elongated die recesses extending along opposing edges of the first surface;

the support paddle includes two spaced apart paddle portions, one received in each of the two elongated die recesses, with each paddle portion being flush with or recessed

from the first surface of the first semiconductor die external to the elongated die recesses;

the first semiconductor die has bond sites accessible from the second surface; and

the second semiconductor die includes two elongated die recesses extending along opposing edges of the third surface of the second semiconductor die

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3. The system of claim 1 wherein the support paddle has a first surface generally flush with or recessed from the first surface of the first semiconductor die external to the recess, and wherein the support paddle has a second surface facing opposite the first surface of the support paddle and toward the first semiconductor die.

4. The system of claim 1 wherein the first semiconductor die includes multiple recesses, and wherein the support paddle includes multiple portions received in individual recesses.

5. The system of claim 4 wherein the first die recess of the first semiconductor die includes a first elongated recess portion positioned along a first edge of the first semiconductor die and a second elongated recess portion positioned along a second edge of the first semiconductor die.

6. The system of claim 5 wherein the support paddle includes a first elongated portion received in the first recess and a second elongated portion received in the second recess.

7. The system of claim 5 wherein the support paddle includes first and second spaced apart portions received in the first recess, and third and fourth spaced-apart portions received in the second recess.

8. The system of claim 1 wherein the first semiconductor die includes a contiguous recess adjacent a periphery of the semiconductor die, and wherein the support paddle includes a

contiguous, generally frame-shaped support surface having a central opening and being received in the contiguous recess of the first semiconductor die.

9. The system of claim 1, further comprising an encapsulant disposed around at least a portion of the semiconductor die and at least a portion of the support paddle.

10. The system of claim 1 wherein the first semiconductor die includes multiple die bond sites, and wherein the system further comprises multiple leadfingers having leadfinger bond sites, with individual leadfinger bond sites connected to corresponding die bond sites via wire bonds, wherein the leadfingers and the support paddle have a generally identical composition.

11. The system of claim 1 wherein the system further comprises:

a plurality of leadfingers having leadfinger bond sites, with individual leadfinger bond sites connected to corresponding die bond sites of the first semiconductor die via wirebonds that are received in the second die recesses of the second semiconductor die.

12. The system of claim 1, further comprising a computing device having at least one of a processor, a memory and an input/output device, and wherein the semiconductor die and the support paddle are included as a component of at least one of the processor, the memory, and the input/output device.

13. A method for manufacturing a semiconductor system, comprising:

receiving at least part of a support paddle in a first recess of a first semiconductor die, the first semiconductor die having a first surface with the first recess and a second surface facing opposite from the first surface;

attaching the support paddle to the first semiconductor die with the support paddle in the first recess;

electrically connecting the leadfingers with bond sites of the semiconductor die using wirebonds; and

attaching a second semiconductor die on the first semiconductor die with an adhesive, the second semiconductor die having a third surface facing the second surface of the first semiconductor die, the third surface having a second recess, wherein a portion of the wirebonds is encapsulated by the adhesive in a space between the second recess and the second surface of the first semiconductor die.

14. The method of claim 13 wherein the support paddle is a portion of a leadframe having a frame portion and a plurality of leadfingers extending from the frame portion, and wherein the method further comprises:

positioning the leadfingers proximate to the first semiconductor die as the support paddle is received in the first recess;

disposing an encapsulant around the first and second semiconductor dies and the leadframe; and

removing the frame portion of the leadframe.

15. The method of claim 13 wherein receiving at least part of the support paddle in the first recess of the first semiconductor die includes receiving the support paddle with an outwardly facing surface of the support paddle flush with or recessed from the first surface of the first semiconductor die adjacent to the first recess.

16. The method of claim 13 wherein the first recess is a first recess portion and wherein receiving at least part of the support paddle includes receiving a first portion of the support paddle in the first recess portion and wherein the method further comprises receiving a second portion of the support paddle in a second recess portion spaced apart from the first recess portion.

17. The method of claim 13 wherein the first recess extends around a periphery of the first semiconductor die, and wherein the support paddle has a support surface with a generally

frame-type shape disposed around a central opening, and wherein the method further comprises positioning a central portion of the first semiconductor die in the central opening of the support paddle.

18. The method of claim 13 wherein the first recess includes at least one recess portion at four spaced apart corners of the first semiconductor die, and wherein receiving at least part of the support paddle in the first recess includes receiving four spaced apart paddle surfaces of support paddle in individual recess portions at the four spaced apart corners of the first semiconductor die.