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PATENT SPECIFICATION

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COMPLETE SPECIFICATION

DRAWINGS ATTACHED

Methods for Fabricating Miniature Semiconductor Devices

We, TEXAS INSTRUMENTS INCORPORATED, of 13500 North Central Expressway, Dallas, Texas, United States of America, a corporation organized and existing under the laws of the State of Delaware, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us. and the method by which it is to be performed, to be particularly described in and by the following statement:

This invention relates to methods for fabricating miniature semiconductor devices. More particularly, it relates to methods for fabricating miniature semiconductor devices from semiconductor materials wherein two or more circuit elements are contained in a unitary structure of semiconductor material, at least two of which circuit elements are passive elements as hereinafter defined.

The present invention is a method of fabricating a miniature semiconductor device having at least two passive circuit elements therein comprising the steps of providing a wafer of single crystal semiconductor material, forming one of said passive circuit elements in one area of said wafer, forming another of said passive circuit elements in another area of said wafer, said steps of forming including the step of masking one major wafer face to define thereon said one and said other areas of said wafer.

The present invention is also a method of fabricating a miniature semiconductor device having at least two passive circuit elements therein comprising the step of providing a wafer of single crystal semiconductor material, forming one of said passive circuit elements are to be formed, and forming an another of said passive circuit elements in another area of said wafer, said steps of forming including the step of masking one major wafer face to define said one and said other of the areas in which the passive elements are to be formed, and forming an isolation volume in the wafer to provide desired isolation between the passive circuit elements through the wafer.

The method of fabricating a semiconductor device according to the invention preferably forms passive circuit elements closely adjacent one major wafer face and in fabricating the device there may be utilized a combination of steps such as diffusion of conductivity type producing ingredients into a semiconductor wafer, masking in order to define predetermined areas of the wafer in which circuit elements are to be formed and mechanical and/or electrical shaping to confine paths for current flow.

Circuit elements within or on the semiconductor wafer may be effectively electrically isolated through the advantageous employment of electrical and/or mechanical shaping.

Shaping includes various ways of obtaining the confined current paths which ways include, as mechanical shaping, the removal of portions of the semiconductor material as by etching, and specialized configuration of the semiconductor material such as long and narrow, "L" shaped, "V" shaped, *etc.*, and which ways further include as electrical shaping, selective conversion of intrinsic semiconductor material by diffusion of impurities thereinto to provide low resistivity paths for current flow and selective conversion of semiconductor material of one conductor-type to the opposite conductivity-type wherein the p-n junction thereby formed acts as a barrier to current flow.

The invention will be apparent from the following more complete discussion of the

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cooperative relationships which exist in the forming, shaping and positioning of the various areas within a wafer of single crystal semiconductor material to produce a miniature semiconductor device susceptible of exploitation in a variety of practical circuit embodiments.

In the accompanying drawings:—

Figures 1 to 5*a* illustrate schematically various circuit components or elements, a number of which may be fabricated in accordance with the present invention in and/or on a wafer of single crystal semiconductor material to be adapted to form at least part of a miniature electrical circuit;

Figure 6*a* illustrates schematically a multivibrator circuit fabricated in accordance with the present invention;

Figure 6*b* shows the wiring diagram for the multivibrator circuit of Figures 6*a* laid out in the same relationship; and

Figure 7 illustrates the wiring diagram of the multivibrator circuit of Figure 6*a* in a more conventional presentation;

Referring now to the drawings in detail, preferred embodiments of the present invention will now be described in detail in order that a better understanding of the invention and the various forms and embodiments of the invention may be obtained.

Figures 1-5 inclusive illustrate in detail circuit elements a number of which can be formed in and/or on a single wafer of semiconductor material in accordance with the present invention. It is noted at this point that the wafer of semiconductor material is of single crystal structure, and can be composed of any suitable semiconductor material. There may be mentioned as example of suitable materials germanium, silicon, intermetallic alloys such as gallium arsenide, aluminium antimonide, indium antimonide, as well as others.

Referring particularly to Figure 1, there is shown a typical design for a resistor which may be formed in a wafer of single crystal semiconductor material with at least one other circuit element. As noted in Figure 1, the design contemplates utilizing the bulk resistance of a body 10 of semiconductor material of either n- or p-type conductivity. Contacts 11 and 12 are made ohmically to one surface of the body 10, spaced apart a sufficient distance to achieve a desired resistance. As will be apparent to one skilled in the art, ohmic connections are those which exhibit symmetry and linearity in terms of resistance to flow of current therethrough in any available direction. If two resistors are to be connecfed together, it is not necessary to provide separate terminations for the common point. The resistance may be calculated from

$$R = \rho L/A$$

where L is the active length in centimetres, A is the cross sectional area, and ρ is the resistivity in ohm-cm of the semiconductor material.

In addition or alternatively to the resistor shown in Figure 1, a resistor may be provided as shown in Figure 1*a* formed as part of a wafer of single crystal semiconductor material. In Figure 1*a*, there is shown a body comprising a region 10*a* of p-type semiconductor material and an n-type region 10*b*. Of course, between the region 10*a* and region 10*b* there is a p-n junction which is designated by the numeral 13. Contacts 11*a* and 12*a* are made to the outside surface of the region 10*b*, spaced apart from each other in order to achieve a desired resistance. As in Figure 1, the contacts 11*a* and 12*a* are ohmic contacts to the region 10*b*. A resistor formed in the manner of Figure 1*a* has several important advantages. First, the p-n junction 13 provides a barrier to current flow from the n-type region 10*b* into the p-type region 10*a* and thus, the current flow is confined to a path in the n-type region 10*b* between the contacts thereto. The second advantage is that the total resistance value thereof can be controlled to a large degree. The total resistance value may be controlled by etching very lightly over the entire surface to remove the uppermost portion of the n-type region 10*b*, being very careful not to etch through the p-n junction. The third, and perhaps major, advantage in forming a resistor according to Figure 1*a* is in that, by controlling the doping level or impurity concentration in the n-type region 10*b*, lower and more nearly constant temperature coefficients may be provided for the resistor.

The above description has been in terms of a p-type region 10*a* and an n-type region 10*b* but is is obvious that the region 10*a* could be equally as well of n-type conductivity and the region 10*b* of p-type conductivity.

Capacitor designs may be obtained by utilizing the capacitance of a p-n junction, as shown in Figure 2, wherein is shown a semiconductor body comprising a region of p-type conductivity and an n-type diffused region 16. Ohmic contacts 17 are made to opposite faces of the body 15, 16. The capacitance of a diffused junction is given by

$$C = A \epsilon \left(\frac{q a}{12 \epsilon V} \right)^{\frac{1}{3}}$$

where A is the area of the junction in square cm, ϵ is the dielectric constant, q is electronic charge, where a is the impurity density gradient and V is the applied voltage.

Instead of the capacitor of Figure 2, capacitance in a body of single crystal semiconductor material may be provided as

shown and described in connection with Figure 2*a*, and which capacitor is the subject of our co-pending patent application No. 5691/62 (Serial No. 945,737). Figure 2*a* shows a body 15*a* of single crystal semiconductor material, of either n-or p-type conductivity, which constitutes one plate of the capacitor. Evaporated onto the body 15*a* is a layer 18 providing a dielectric layer for the capacitor. It is necessary that the layer 18 have a suitable dielectric constant and be inert when in contact with the semiconductor body 15*a*. Silicon dioxide has been found to be a suitable material for dielectric layer 18 and may be applied by evaporation or thermal oxidation techniques onto body 15a. Plate 19 forms the other plate of the capacitor and is provided by evaporating a conductive material onto layer 18. Gold and aluminium have been found to be satisfactory materials for the plate 19. Ohmic contact 17 is made to the body of semiconductor material 15*a* and contact to plate 19 may be made by any suitable electrical contact (not shown). Capacitors formed in the manner described in connection with Figure 2*a* have been found to exhibit much more stable characteristics than pure junction capacitors, that is, p-n junction capacitors.

Capacitors produced in the manner of Figure 2 are also diodes, and must therefore be properly polarized in the circuit. Nonpolar capacitors may be made by connecting two such area back-to-back. Although junction capacitors have a marked voltage dependence, such dependence is present to a lesser degree for low voltages in the nonpolar configuration.

Resistor and capacitor designs may be combined to form a distributed R-C network. Such is shown in Figure 3, wherein a body comprising a region 20 of p-type conductivity has an n-type conductivity diffused region 21 formed therein. A broad area contact 22 is placed on the diffused region on one face of the body and spaced contacts 23 on the opposite face of the body. These networks are useful for low pass-filters, phase shift networks, coupling elements, *etc.* Their parameters may be calculated from the equations above. Other configurations of the general type are also possible.

As shown in Figures 4 and 5, transistors and diodes may be formed on or in a single wafer. In Fig. 4, the transistor has a collector region 25, a diffused p-n junction 26, a base layer 27, an emitter contact 28 forming a rectifying connection with base layer 27 and base and collector contacts 29 and 30, respectively. The base layer 27 is formed as a mesa of small cross section. A diode of similar design is shown in Figure 5, and consists of region 35 of one type conductivity, and a mesa region 36 of opposite conductivity-type with p-n diffused junction formed therebetween and contacts 37 and 48 connected to each region.

Small inductances, suitable for high frequency use, may also be made by shaping the semiconductor as evidenced by Figure 5*a*, which shows a spiral of semiconductor material. It is also possible to prepare photosensitive devices including photovoltaic cells, photoresistors and solar cells and other like components utilizing the basic design considerations hereinbefore outlined.

Although all of the circuit elements have been described in terms of a single diffused layer, it is quite possible where practical, to use a double diffused structure. Thus ,double diffusion may be employed to form both n-p-n and p-n-p transistor structures, for example: Moreover, any suitable materials can be used for the semiconductor materials, conductivity producing impurities, and contact materials ; and suitable and known processing can be exploited to produce circuit element designs.

Because all of the circuit element designs described above can be formed from a single material, a semiconductor, it is possible by shaping to integrate all of them into a single crystal semiconductor wafer and to process the wafer to provide the proper network and the correct circuit element values.

As will be apparent to one skilled in the art, circuit elements can be classified according to their circuit functions. Thus, circuit elements may be thought of as being either active or passive in nature. Active elements are those which in an impedance network act as current generators; whereas passive elements do not so act, and the term "Active element(s)" and "passive element(s)" where used hereinafter and in the claims are to be construed in this sense. Examples of active elements are photovoltaic cells and transistors ; and examples of passive elements are resistors, capacitors and inductors. Elements which fall into the general category of diodes and are normally employed as passive elements, may if suitably biased and energized, function in an active nature.

A specific illustration of an electronic circuit fabricated in accordance with the invention is shown in Figure 6*a*. As shown, a thin wafer of single crystal semiconductor material containing a p-n junction formed between two monocrystalline layers which wafer has been processed and shaped to include discrete areas adapted to provide the electrical properties of circuit elements forming a complete and integrated multivibrator electronic circuit closely adjacent one major wafer face. The regions of the

wafer have been marked with symbols representative of the circuit element functions that are performed in the various regions. Figure 6*b* shows a wiring diagram of the various circuit functions in the relationship which they occupy in the wafer of Figure 6*a*. A more conventionally drawn circuit diagram is shown in Figure 7 with the circuit values actually used. The multivibrator circuit shown in Figures 6*a*, 6*b* and 7 will be described as illustrative of the processing techniques required. First, a wafer of single crystal semiconductor material, preferably silicon or germanium, of the proper resistivity is tapped and polished on one side. For this design, 3 ohm-cm p-type germanium was used. The wafer was then subjected to an antimony diffusion process which produced a monocrystalline n-type layer on the surface about 0.7 mils deep. The wafer was then cut to the proper size, 0.200 x 080 inches, and the unpolished surface lapped to give a wafer thickness of 0.0025 inches.

Gold plated Kovar (Registered Trade Mark) leads 50 were attached by alloying to the wafer in the proper positions. Kovar is a trade name for an iron-nickel-cobalt alloy. Gold was then evaporated through a mask to provide the areas 51-54 which provide ohmic contact with the n region, such as the transistor base connections and the capacitor contacts. Aluminium was evaporated through a properly shaped mask to provide the transistor emitter areas 56, which form rectifying contacts with the n layer. Alternatively a p-type conductivity producing ingredient may be diffused through a properly shaped mask to provide the transistor emitter areas 56. Suitable ohmic contacts may be secured to the emitter areas in the same manner as the securing of contacts 53 and 54 to base areas of transistors T_2 and T_1. When the emitter area is formed either by diffusion or alloying a monocrystalline layer of conductivity type opposite to that of the base region is provided. The monocrystalline layers of the base and emitter regions are contiguous and form therebetween a p-n junction extending to the major wafer face and there defining an enclosed area of semiconductor material.

In the completed device the p-n junction formed between the collector and base regions also extends to the major wafer face and there defines an enclosed area of semiconductor material surrounding the first mentioned enclosed area.

The wafer was then coated with a photosensitive resist or lacquer, such as Eastman (Registered Trade Mark) Photo Resist, supplied by Eastman Kodak Company, and exposed through a negative to a light. The lacquer image remaining after development was used as a resist for etching the wafer to the proper shape. In particular, this etching forms a slot through the wafer to provide an isolation volume between R_1 and R_2 thereby electrically isolating R_1 and R_2 from each other along at least a major part of their lengths and from the rest of the circuit elements. This etching also shapes all of the resistor areas to the previously calculated configuration. Either chemical etching or electrolytic etching may be used, although electrolytic etching appears to be preferable.

After this step, the photoresist was removed with a solvent, and the areas 60, and such other areas as necessary, for example the capacitor areas C_1 and C_2 were masked by the same photographic process. The wafer was again immersed in etchant, and the n layer completely removed in the exposed areas thereby forming the mesa shapes. A chemical etch is considered preferable. The photoresist was then removed.

Reference is herein made to our co-pending patent applications Nos. 28004/63 and28005/63 (Serial Nos. 945747 and 945748) and our co-pending patent applications Nos. 27197/63 and 27540/63 (Serial Nos. 945741 and 945744) to illustrate various forming techniques within the scope of the invention.

Although Fig. 6*a* has been described embodying resistors according to Fig. 1, it will be manifest that these resistors may be constructed according to Fig. 1a, i.e. diffused resistors may be substituted, where desired and practical, for the bulk resistors illustrated.

Gold wires 70 were then thermally bonded to the appropriate areas to complete the connections, and a final clean-up etch given. Instead of using the gold wires 70 in making electrical connections, connections may be provided in other ways. For example, in accordance with the invention described in our co-pending patent application No. 3836/63 (Serial No. 945738) an insulating and inert material such as silicon oxide may be evaporated onto the semiconductor circuit wafer through a mask either to cover the wafer completely except at the points where electrical contact is to be made thereto, or to cover only selected portions joining the points to be electrically connected. Electrically conducting material such as gold may then be laid down on the insulating material to make the necessary electrical circuit connections.

After testing, the circuit may be hermetically sealed, if required, for protection against contamination. The finished device was smaller by several orders of magnitude than any others which have previously been proposed. Because the fabrication

steps required are quite similar to those now used in manufacturing transistors, and because of the relatively small number of steps required, these devices are inherently inexpensive and reliable, as well as compact.

It must be emphasised that the embodiments described above are merely examples of inumerable networks which can be fabricated utilizing the technique of the present invention. There is no limit upon the complexity of configuration of circuits which can be made in this manner, for example any desired cooperative combination of selected circuit elements as hereinbefore described with reference to Figs. 1 to 5 may be embodied in a single wafer to form a network and the network may be such that upon the application of electrical power, there is performed within the structure an electrical function performed by a plural element electrical network.

Reference is additionally made to our co-pending parent patent application No. 3633/60 (Serial No. 945734) and to our patent applications Nos. 27542/63; 27196/63; 27195/63; 27198/63; 32744/63; and 27541/63 (Serial Nos. 945746, 945740, 945739, 945742, 945749 and 945745) also divided from the parent application.

Terms indicative of position, such as "on," are used in the following claims to define relationship of parts in a form convenient for the purpose, but such terms are not to be construed in any restrictive sense and it will be manifest that the semiconductor devices could be utilized in any desired positional orientation.

WHAT WE CLAIM IS:—

1. A method of fabricating a miniature semiconductor device having at least two passive circuit elements therein comprising the steps of providing a wafer of single crystal semiconductor material, forming one of said passive circuit elements in one area of said wafer, and forming another of said passive circuit elements in another area of said wafer, said steps of forming including the step of masking one major wafer face to define thereon said one and said other areas of said wafer.

2. A method of fabricating a miniature semiconductor device according to claim 1, wherein said steps of forming include the step of diffusion to introduce a conductivity-type producing ingredient into said wafer.

3. A method of fabricating a miniature semiconductor device according to claim 2, including the step of mechanically or electrically shaping the wafer to provide through the wafer the desired isolation between selected elements.

4. A method of fabricating a miniature semiconductor device according to claim 2, wherein the step of diffusion in each step of forming of the passive circuit elements is concurrent with the other or another.

5. A method of fabricating a miniature semiconductor device according to any preceding claim, wherein the region immediately underlying each of said passive circuit elements has a conductivity type opposite to that of the contiguous region of the corresponding passive circuit element.

6. A method of fabricating a miniature semiconductor device according to any preceding claim, including the step of positioning a plurality of electrical contacts on said wafer ohmically connected to said passive circuit elements.

7. A method of fabricating a miniature semiconductor device having at least two passive circuit elements therein comprising the steps of providing a wafer of single crystal semiconductor material, forming one of said passive circuit elements in one area of said wafer, forming another of said passive circuit elements in another area of said wafer, said steps of forming including the step of masking one major wafer face to define said one and said other of the areas in which the passive elements are to be formed, and forming an insulating volume in the wafer to provide through the desired isolation between the passive circuit elements.

8. A method of fabricating a miniature semiconductor device according to claim 7, wherein each step of forming includes the step of diffusion to introduce a conductivity-type producing ingredient into said wafer.

9. A method of fabricating a semiconductor device according to claim 8, wherein the step of diffusion in each step of forming is concurrent with the other or another.

10 A method of fabricating a miniature semiconductor device according to any of claims 7 to 9, wherein the region immediately underlying each of said passive circuit elements has a conductivity type opposite to that of the contiguous region of the corresponding passive circuit element.

11. A method of fabricating a miniature semiconductor device according to any of claims 7 to 10, including the step of positioning a plurality of electrical contacts on said wafer each ohmically connected to a respective one of said passive circuit elements.

12. A miniature semiconductor device when produced by the method of any preceding claim.

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It must be emphasised that the embodiments described above are merely examples of inumerable networks which can be fabricated utilizing the technique of the present invention. There is no limit upon the complexity of configuration of circuits which can be made in this manner, for example any desired cooperative combination of selected circuit elements as hereinbefore described with reference to Figs. 1 to 5 may be embodied in a single wafer to form a network and the network may be such that upon the application of electrical power, there is performed within the structure an electrical function performed by a plural element electrical network.

Reference is additionally made to our co-pending parent patent application No. 3633/60 (Serial No. 945734) and to our patent applications Nos. 27542/63; 27196/63; 27195/63; 27198/63; 32744/63; and 27541/63 (Serial Nos. 945746, 945740, 945739, 945742, 945749 and 945745) also divided from the parent application.

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2. A method of fabricating a miniature semiconductor device according to claim 1, wherein said steps of forming include the step of diffusion to introduce a conductivity-type producing ingredient into said wafer.

3. A method of fabricating a miniature semiconductor device according to claim 2, including the step of mechanically or electrically shaping the wafer to provide through the wafer the desired isolation between selected elements.

4. A method of fabricating a miniature semiconductor device according to claim 2, wherein the step of diffusion in each step of forming of the passive circuit elements is concurrent with the other or another.

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6. A method of fabricating a miniature semiconductor device according to any preceding claim, including the step of positioning a plurality of electrical contacts on said wafer ohmically connected to said passive circuit elements.

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8. A method of fabricating a miniature semiconductor device according to claim 7, wherein each step of forming includes the step of diffusion to introduce a conductivity-type producing ingredient into said wafer.

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