

Figure 1

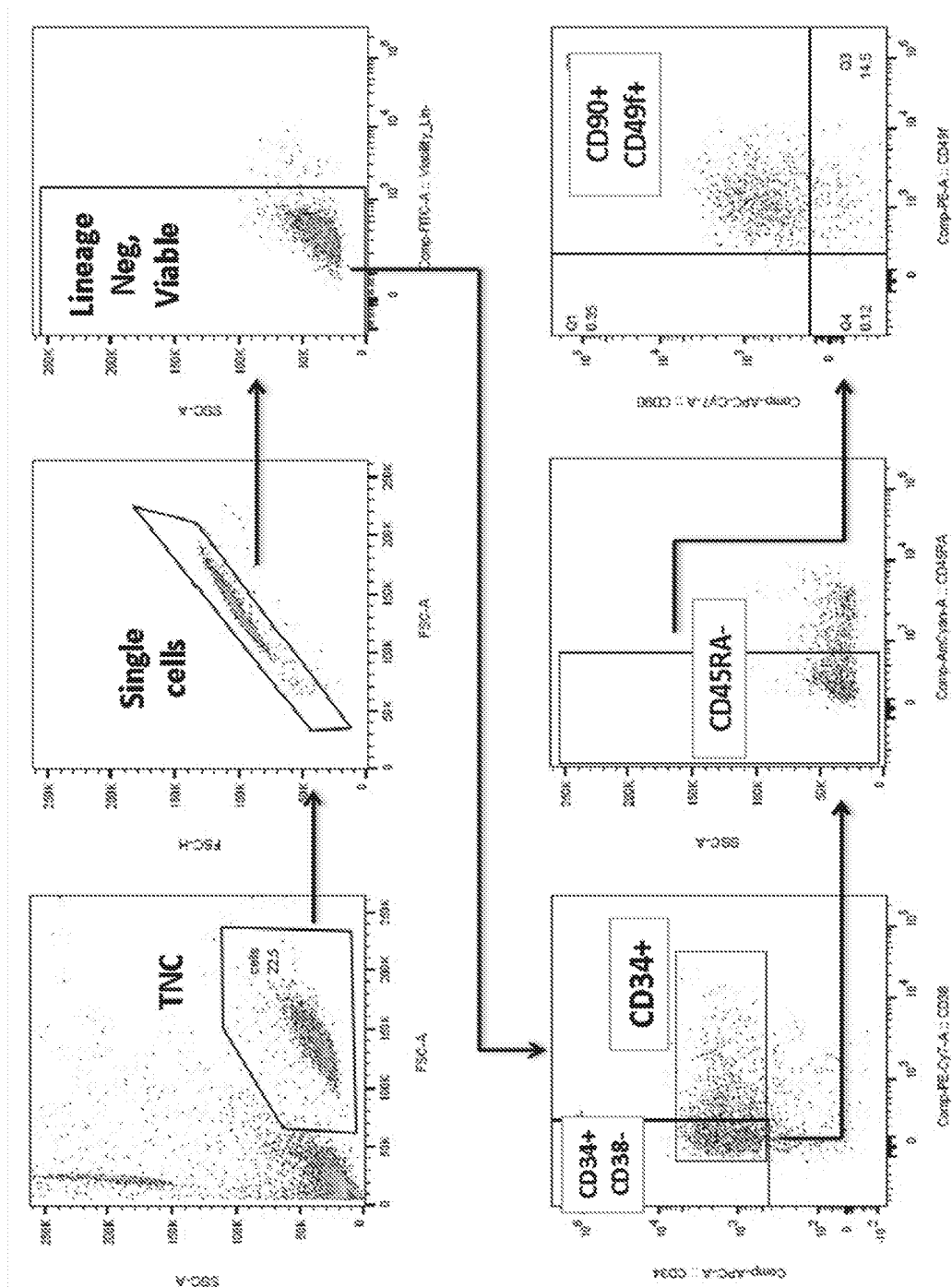


Figure 2A

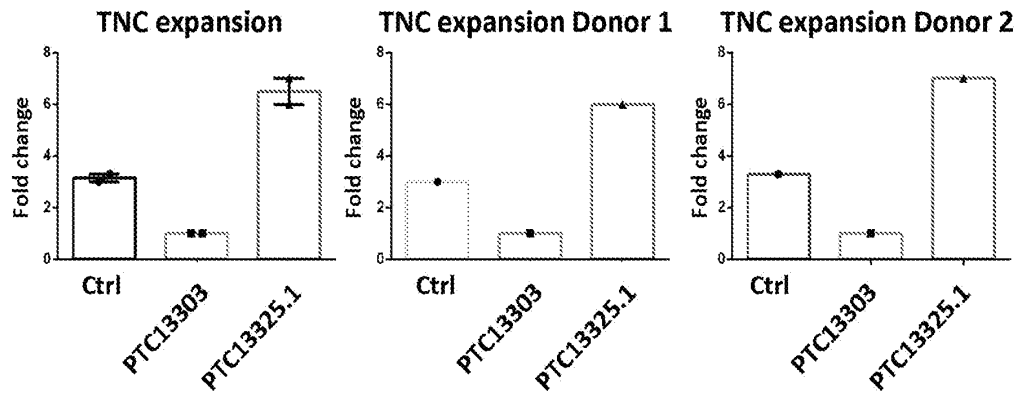


Figure 2B

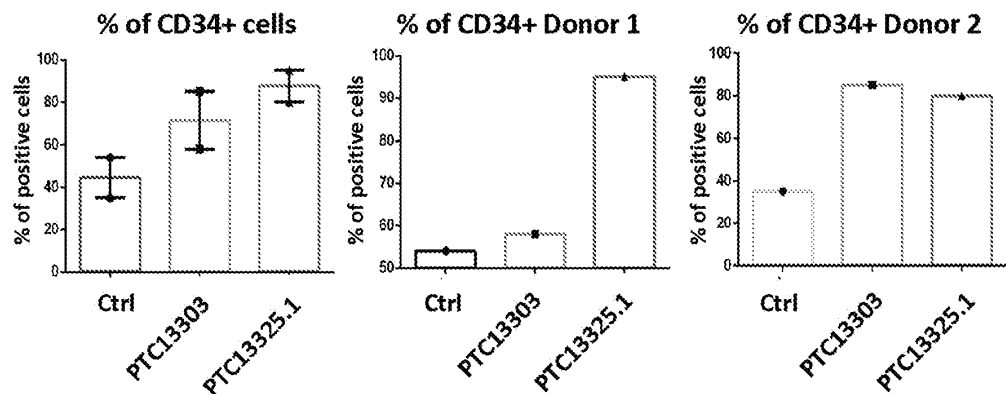


Figure 2C (i)

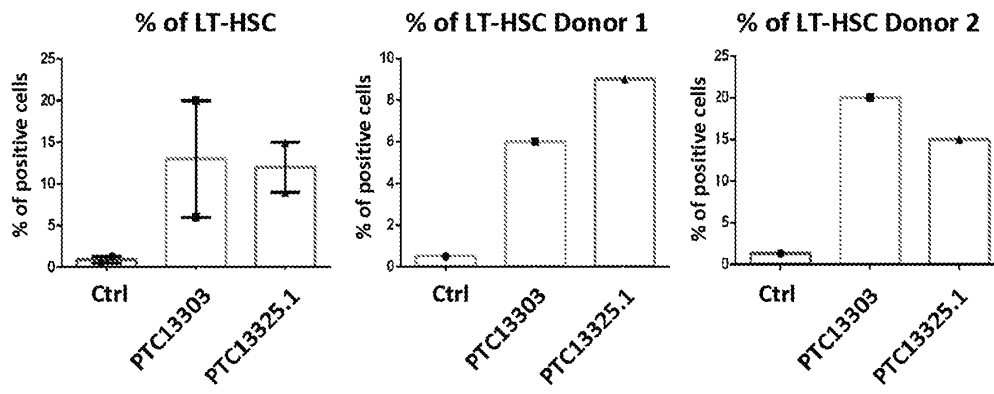


Figure 2C (ii)

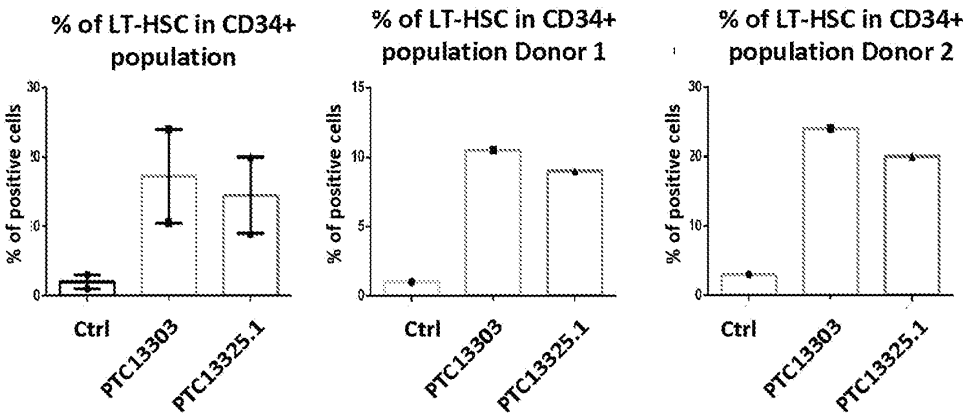


Figure 2D

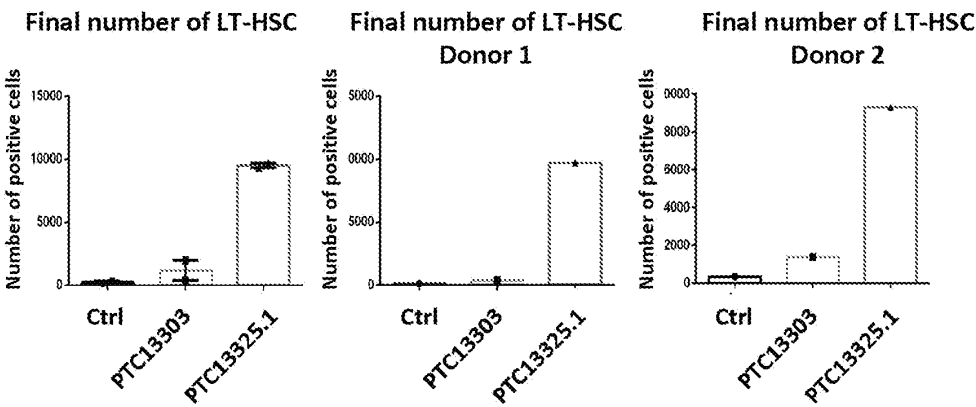


Figure 2E (i)

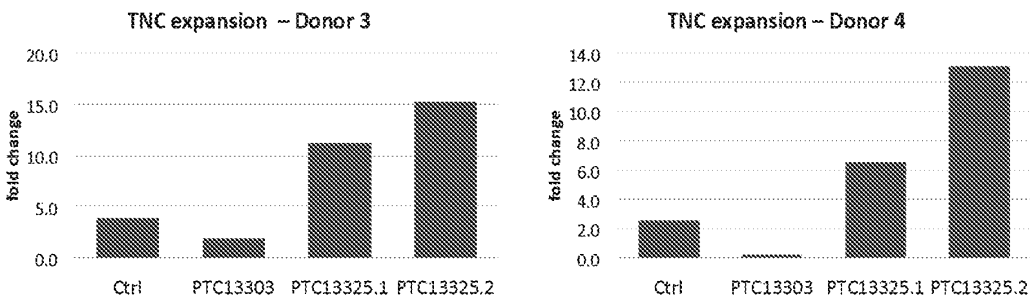


Figure 2E (ii)

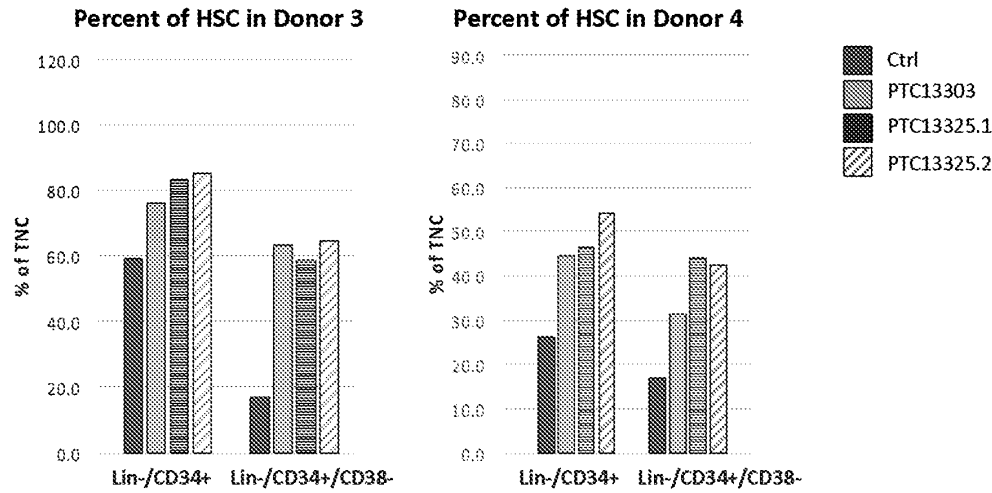


Figure 2E(iii)

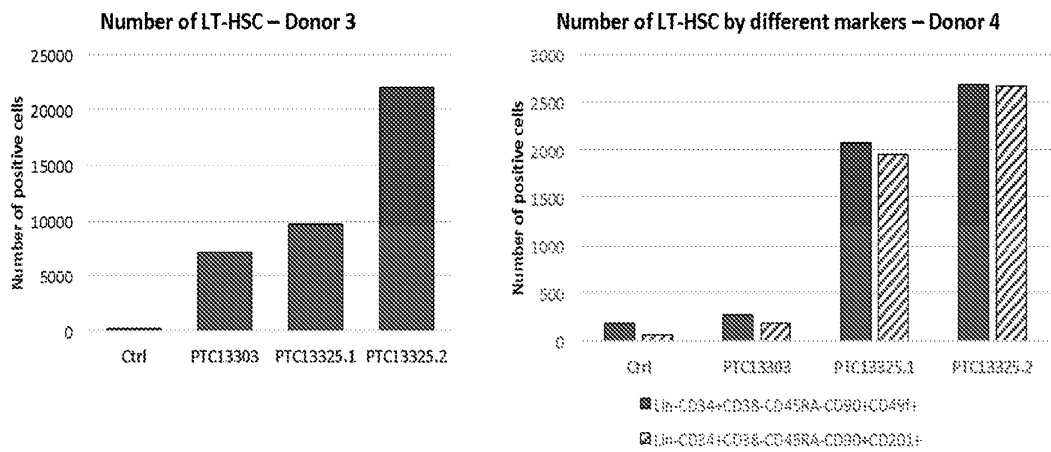


Figure 2E(iv)

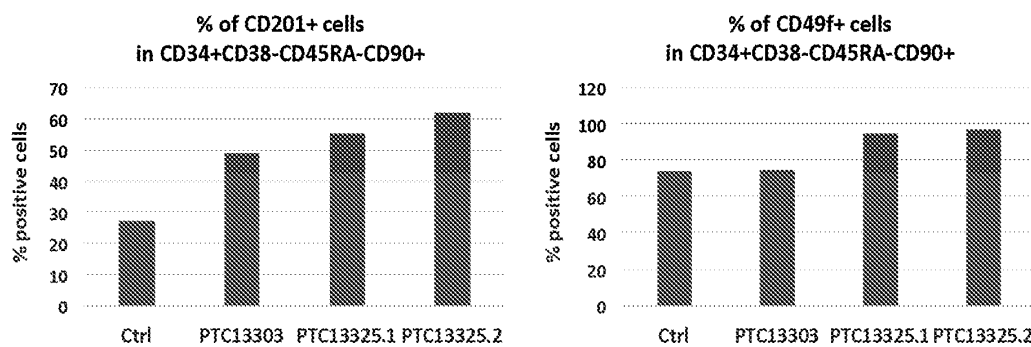


Figure 2F

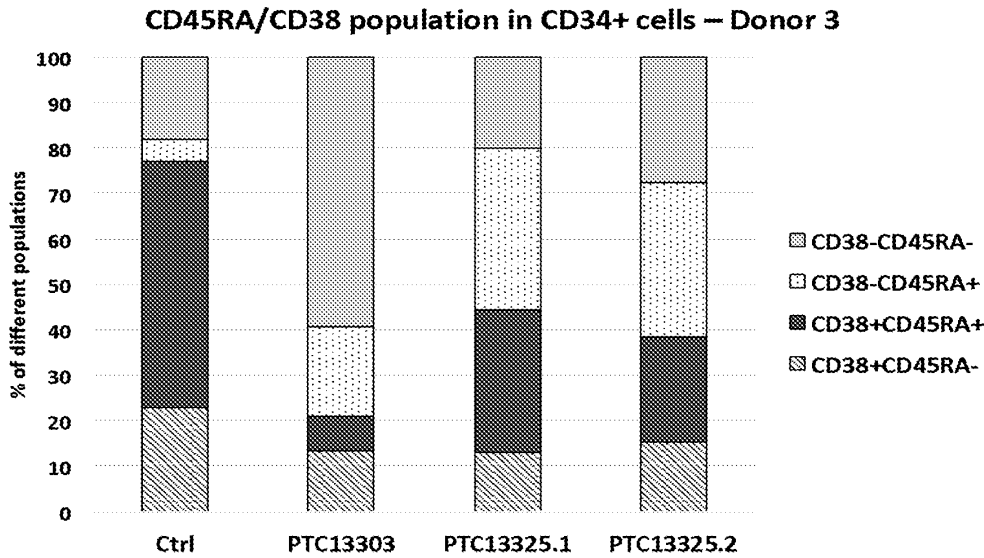


Figure 3(i)

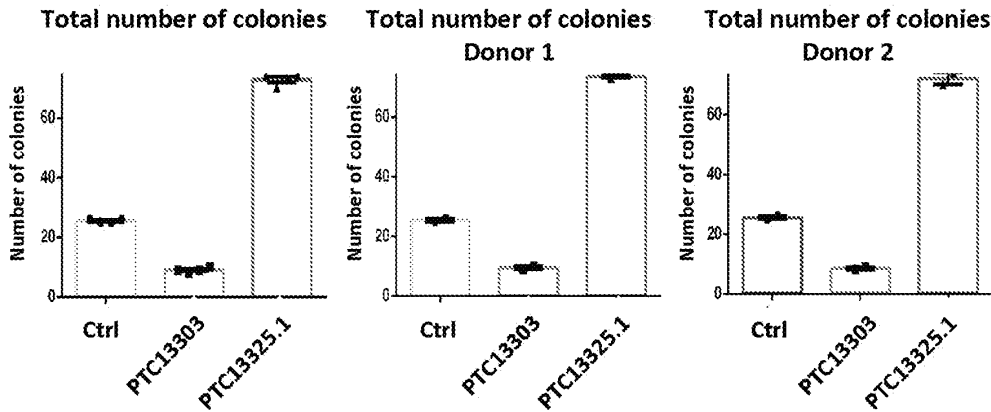


Figure 3(ii)

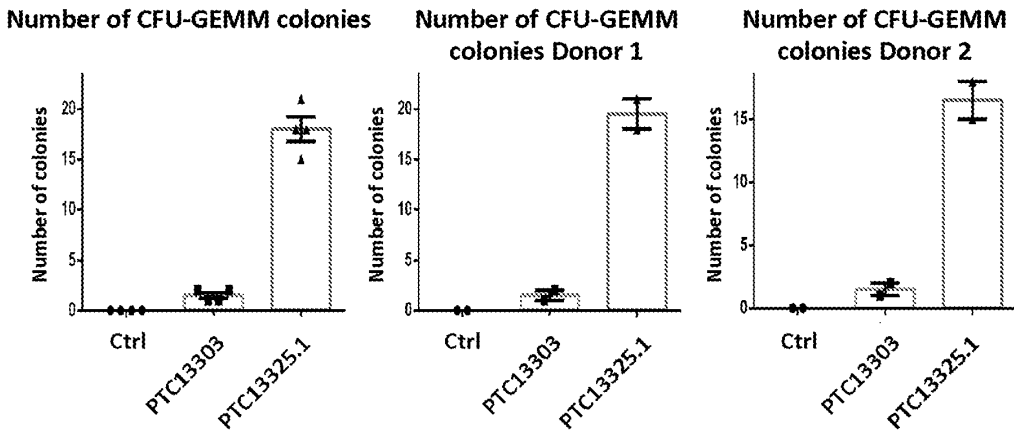
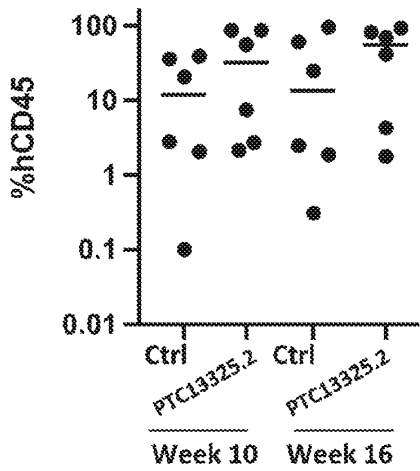


Figure 4A

(i)



(ii)

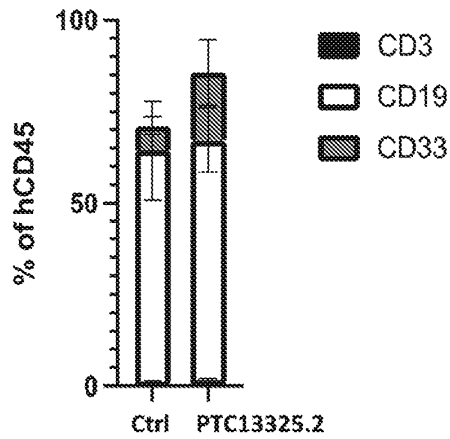
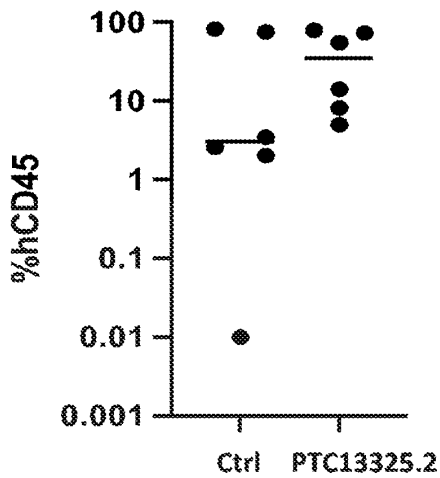


Figure 4B

(i)



(ii)

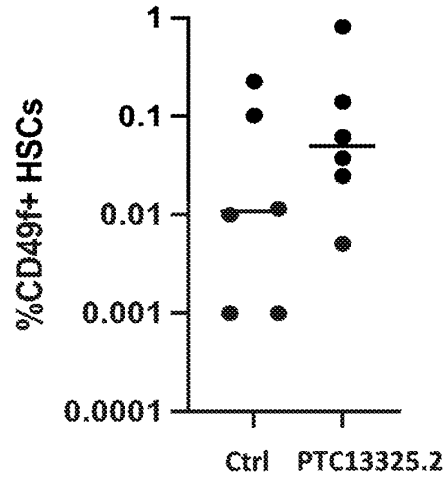


Figure 5

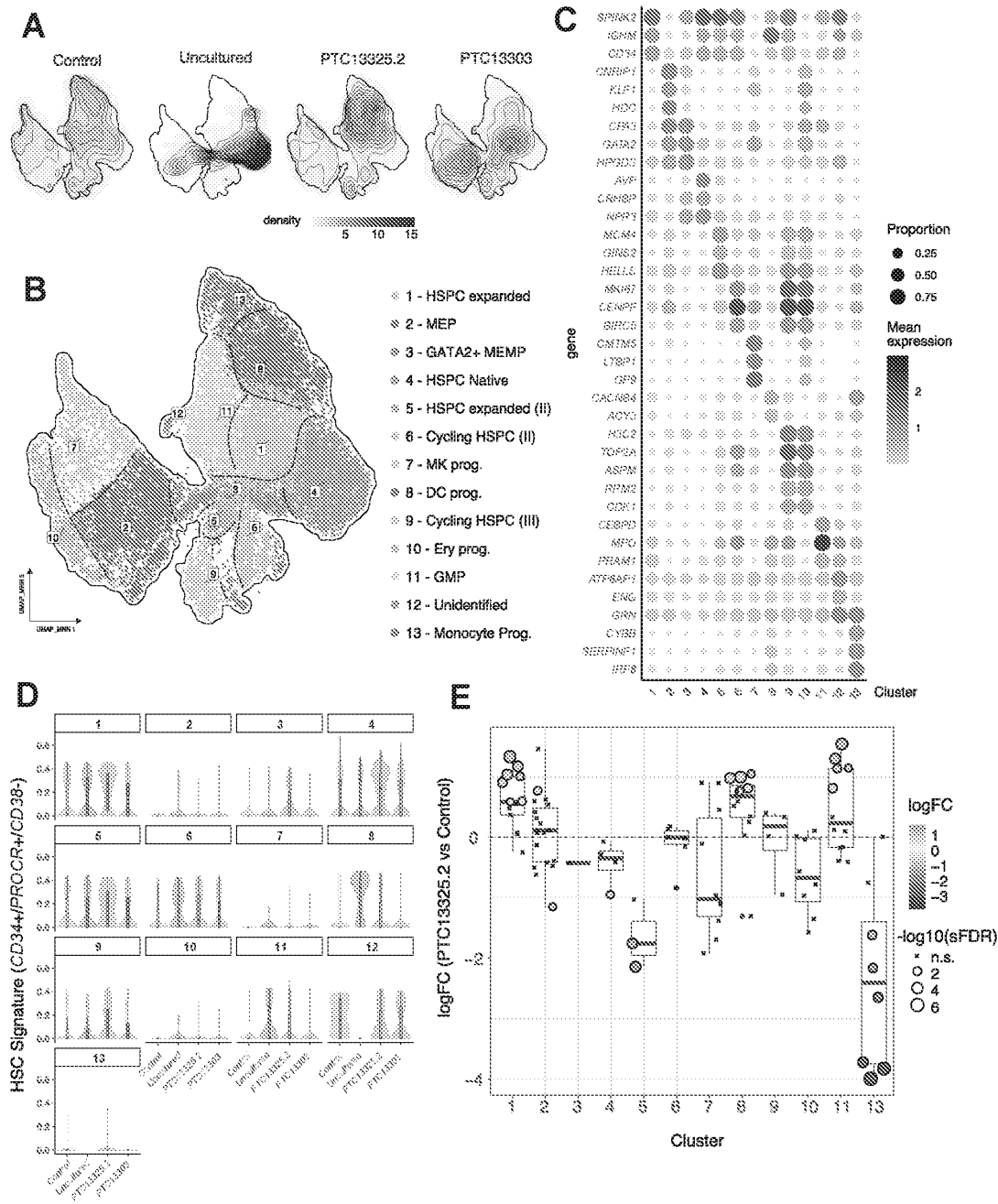


Figure 6A

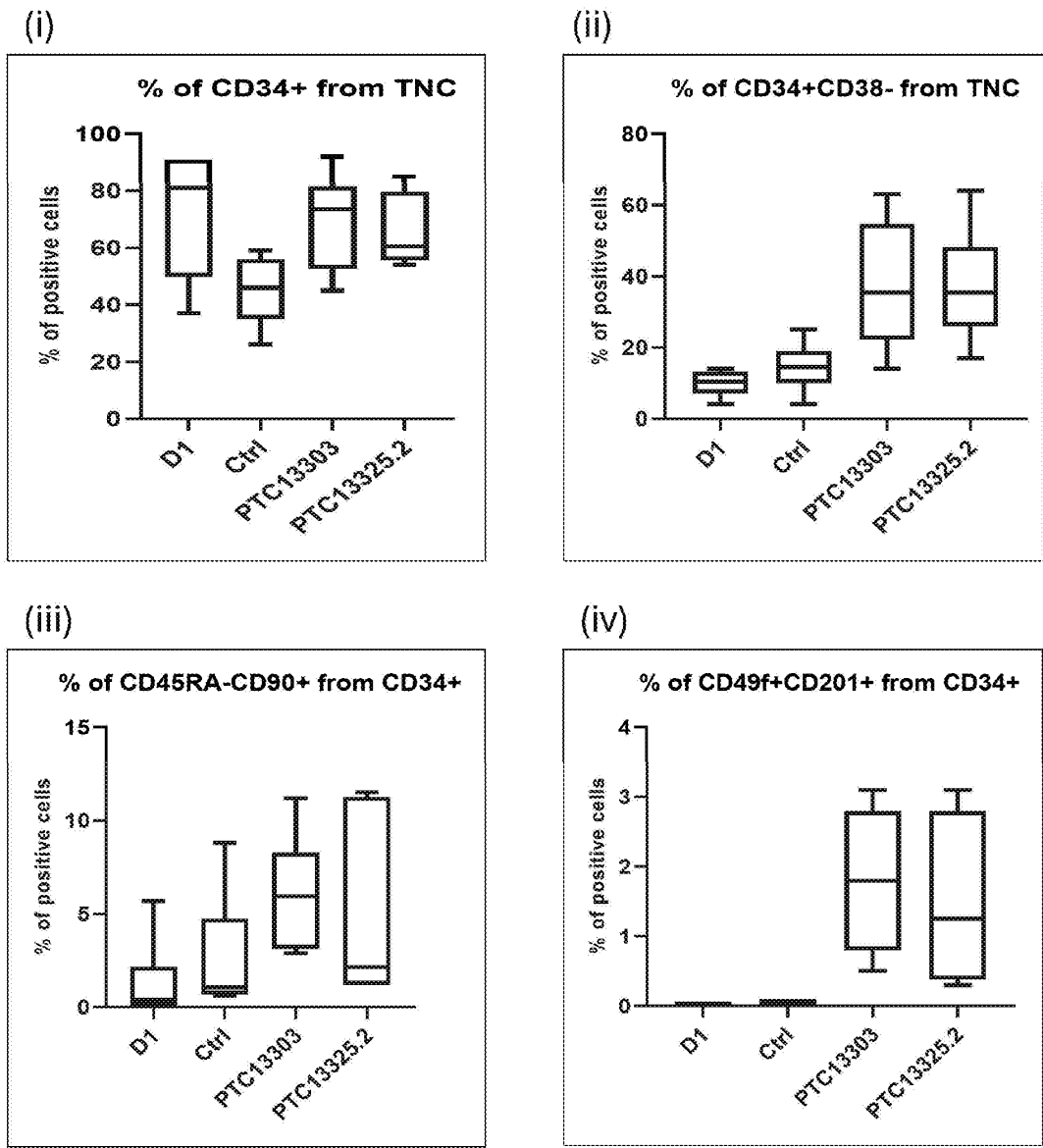


Figure 6B

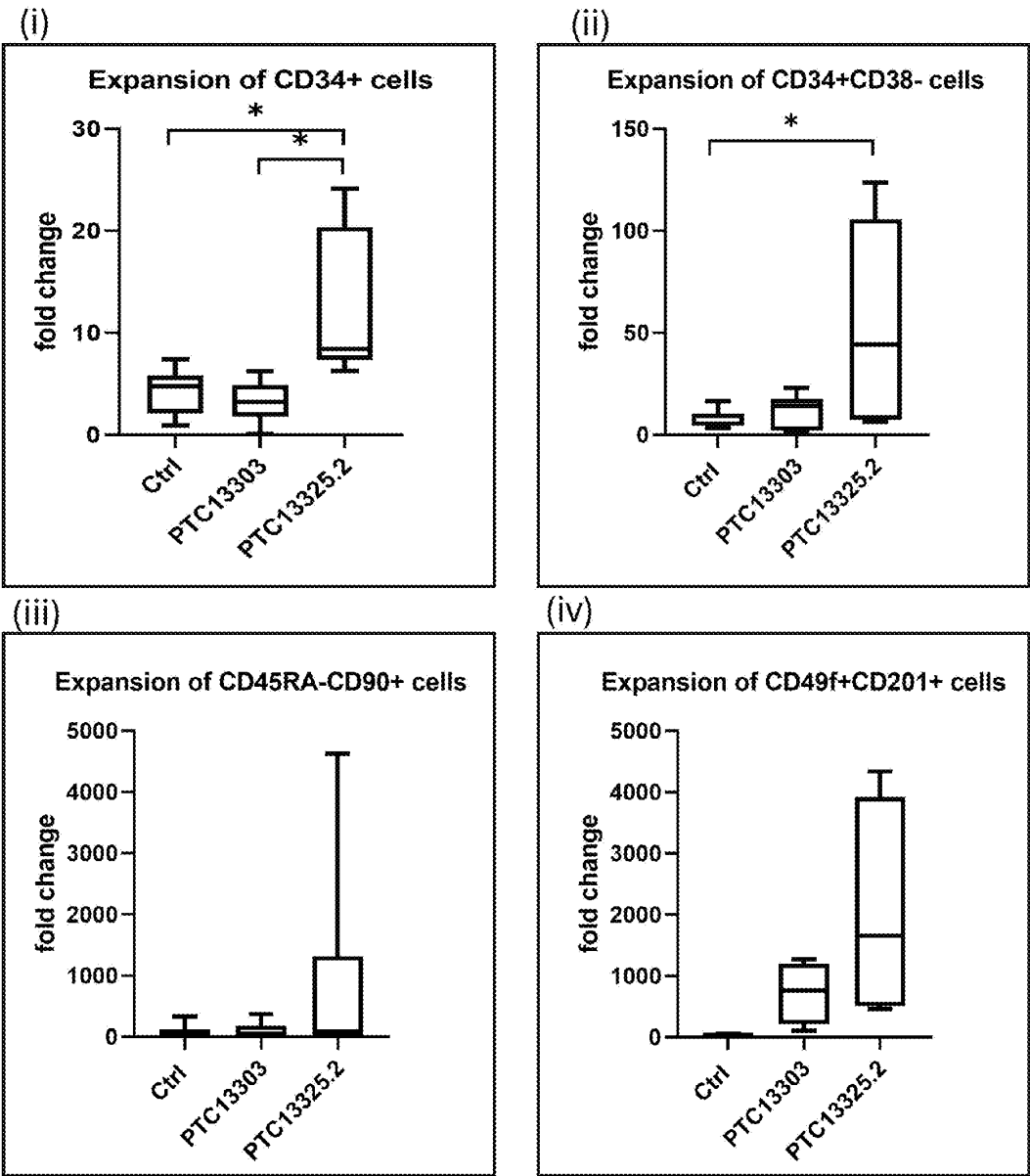
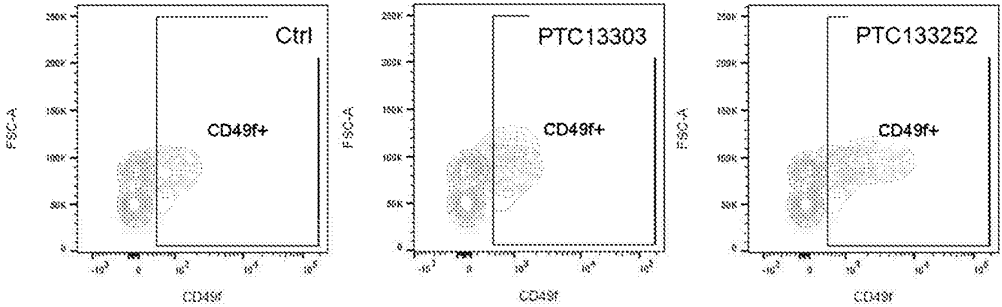


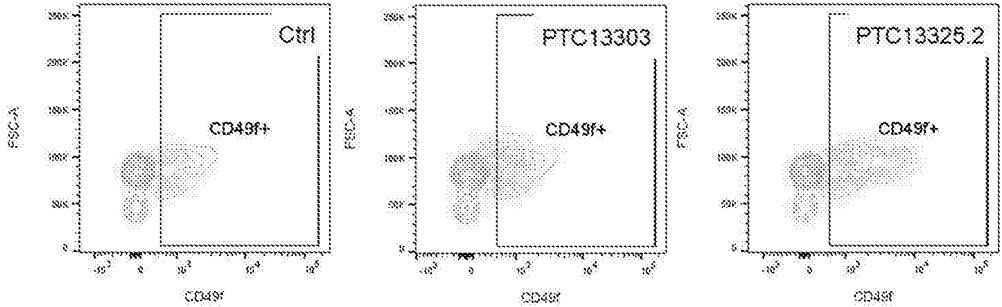
Figure 6C

(i)

Gated on Lin-CD34+CD38-CD45RA-CD90+



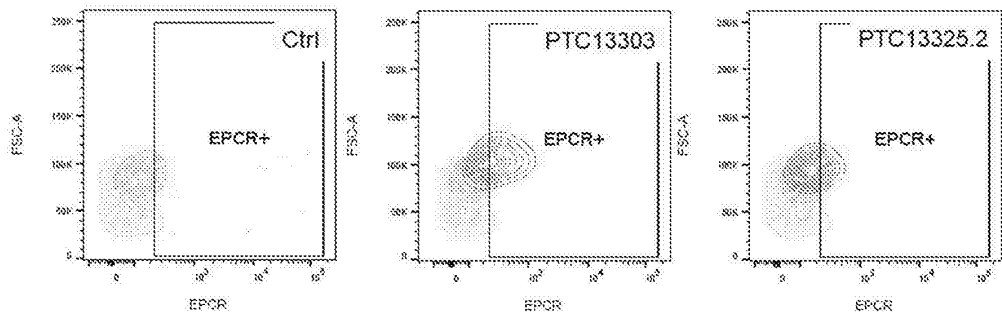
Gated on Lin-CD34+CD38-CD45RA-CD90-



EPCR

(ii)

Gated on Lin-CD34+CD38-CD45RA-CD90+



Gated on Lin-CD34+CD38-CD45RA-CD90-

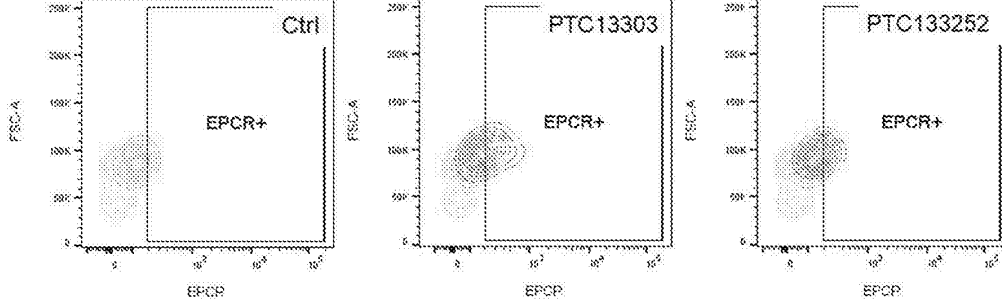


Figure 7A

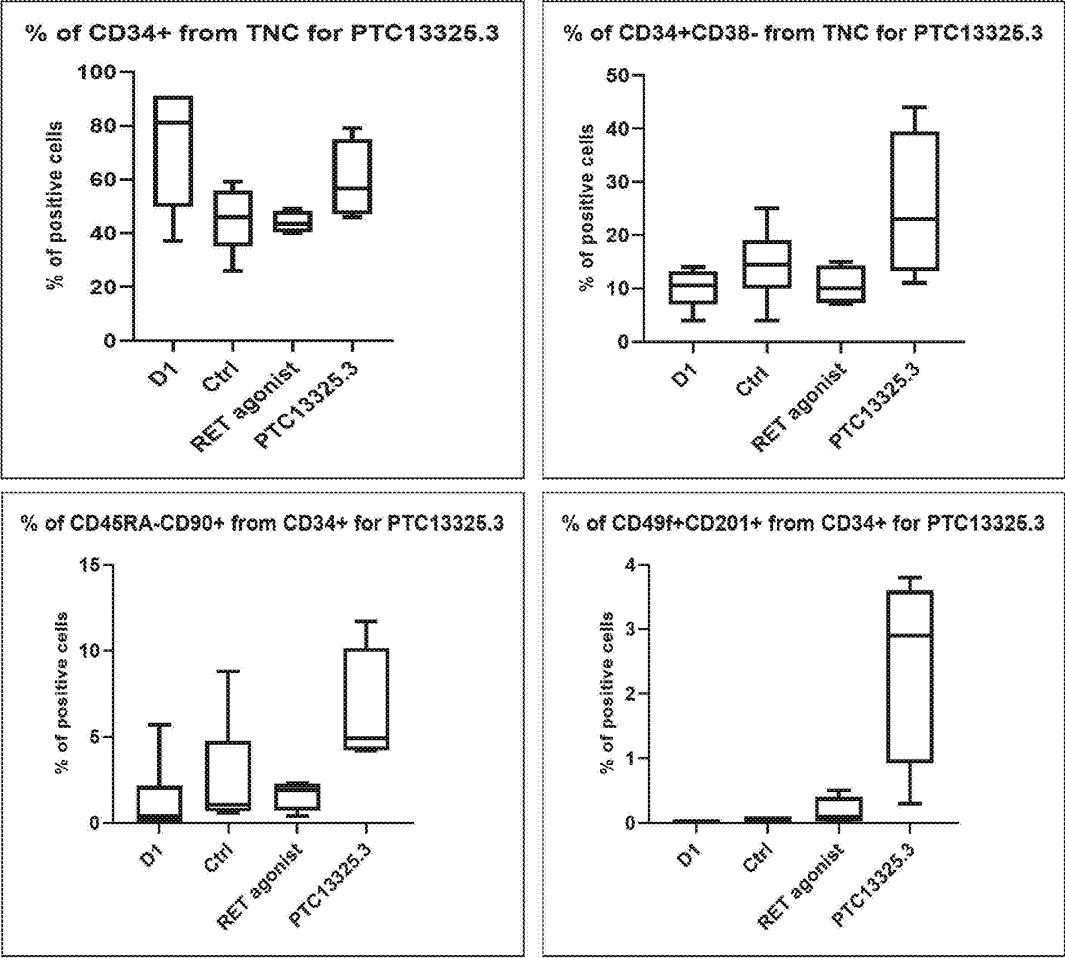


Figure 7B

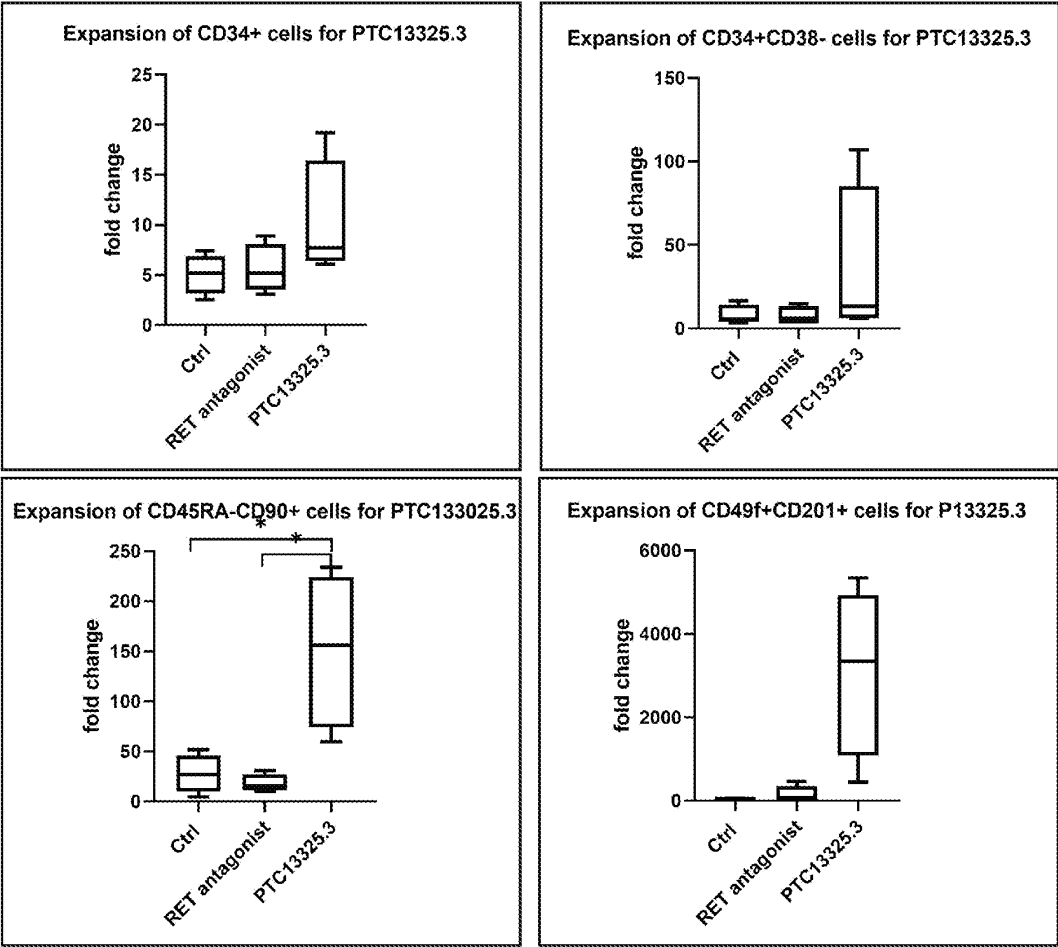


Figure 7C

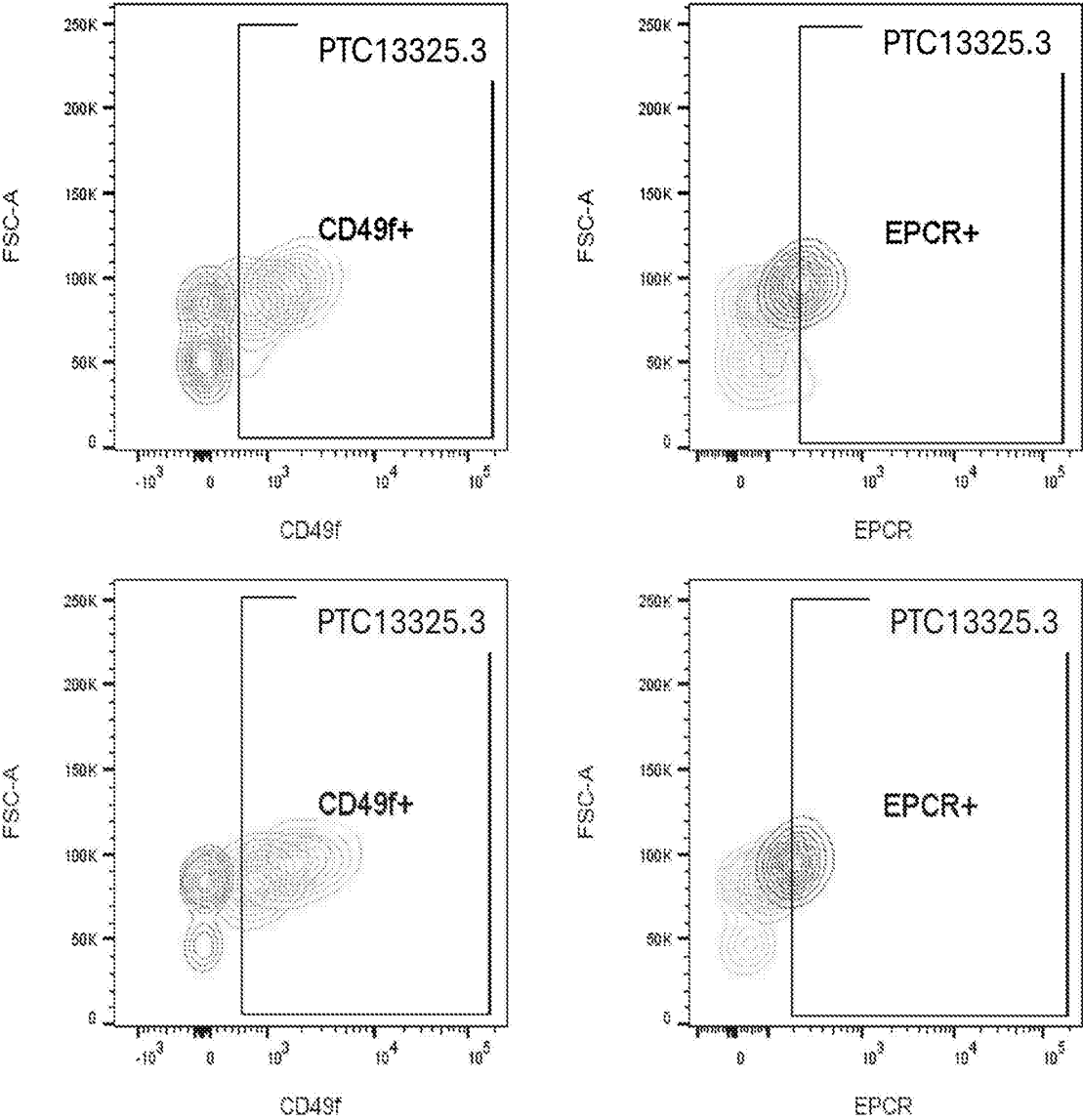


Figure 7D

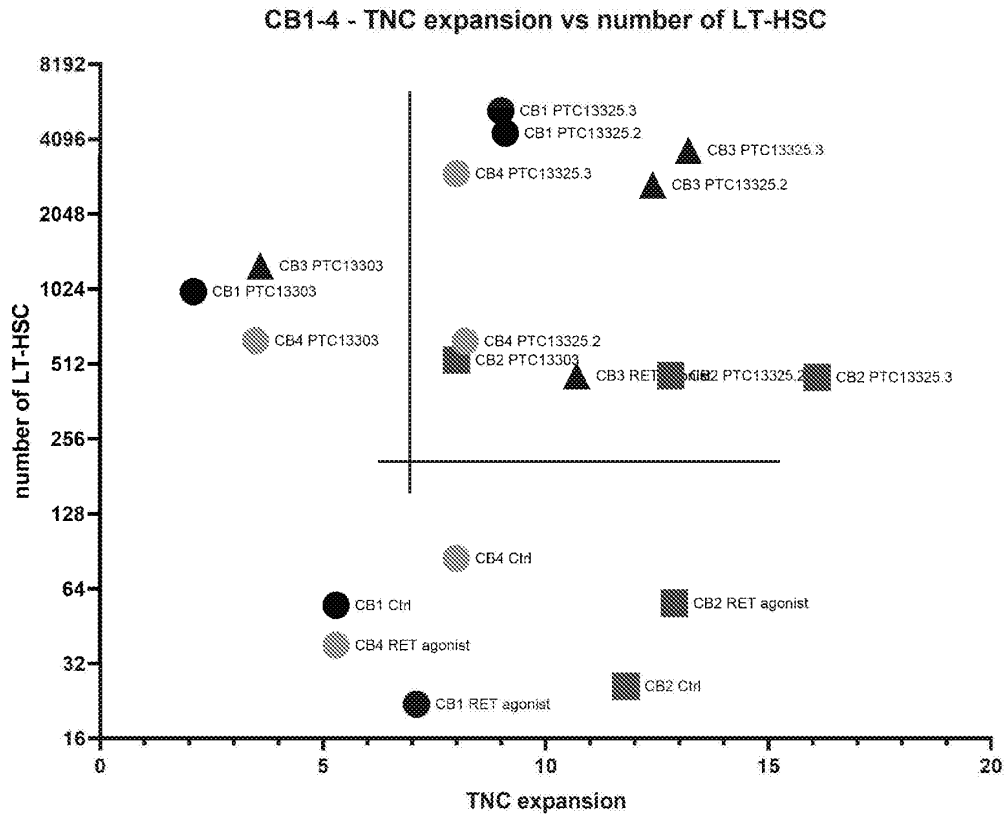


Figure 7E

