ABSTRACT

METHOD OF FABRICATING T-SHAPED RECESSED POLYSILICON GATE TRANSISTORS

A method of fabricating a semiconductor transistor device comprising the following steps. A semiconductor structure is provided having an upper silicon layer, a pad dielectric layer over the upper silicon layer, and a well implant within a well region in the upper silicon layer. A lower SiN layer is deposited and patterned over the pad dielectric layer to define a lower gate area. The pad dielectric layer and the upper silicon layer within the lower gate area is etched to form a lower gate trench having a predetermined width. A lower gate portion is formed within the lower gate trench. An upper oxide layer is formed over the lower SiN layer. An upper SiN layer is formed over the upper oxide layer. The upper SiN layer is etched to define an upper gate trench having a predetermined width greater than the lower gate trench predetermined width. An upper gate portion is formed within the upper gate trench, wherein the lower and upper gate portions form a T-shaped gate. The etched upper SiN, upper oxide, and lower SiN layers are removed to expose the T-shaped gate extending above the pad dielectric layer. An uppermost oxide layer is formed over the exposed T-shaped gate. SiN sidewall spacers are formed adjacent the exposed vertical side walls of the lower polysilicon gate portion. Silicide regions are formed over the T-shaped gate and source/drain regions.

Fig 2