

PLASMA PROCESSING APPARATUS AND RING ASSEMBLY

FIELD

[0001] Exemplary embodiments of the present disclosure relate to a plasma processing
5 apparatus and a ring assembly.

BACKGROUND

[0002] Patent Literature 1 describes a method for surface finishing a component useful for
a plasma processing apparatus.

10 CITATION LIST

PATENT LITERATURE

[0003] Patent Literature 1: U.S. Patent Application Publication No. 2004/0238487

BRIEF SUMMARY

15 TECHNICAL PROBLEM

[0004] The present disclosure provides a technique for reducing particle generation.

SOLUTION TO PROBLEM

[0005] A plasma processing apparatus according to one exemplary embodiment of the
20 present disclosure includes a chamber, a substrate support, a first ring member, and a second
ring member. The substrate support is located in the chamber and includes a substrate support
surface to support a substrate. The first ring member is located on the substrate support and
surrounds the substrate support surface. The first ring member has a first surface roughness.
The first ring member is conductive. The second ring member is located on the substrate
25 support and surrounds the first ring member. The second ring member is insulating. At least
a part of a surface of the second ring member has a second surface roughness greater than the
first surface roughness. The second surface roughness is 4 to 8 μm inclusive.

ADVANTAGEOUS EFFECTS

[0006] The technique according to one exemplary embodiment of the present disclosure can reduce particle generation.

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BRIEF DESCRIPTION OF DRAWINGS

[0007] FIG. 1 is a diagram of a plasma processing system, illustrating an example structure.

FIG. 2 is a diagram of a capacitively coupled plasma processing apparatus, illustrating an example structure.

FIG. 3 is an enlarged partial view of a ring assembly 112 in an example structure.

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FIG. 4 is a flowchart of an example plasma processing method.

DETAILED DESCRIPTION

[0008] One or more embodiments of the present disclosure will be described below.

[0009] In one exemplary embodiment, a plasma processing apparatus is provided. The plasma processing apparatus includes a chamber, a substrate support, a first ring member, and a second ring member. The substrate support is located in the chamber and includes a substrate support surface to support a substrate. The first ring member is located on the substrate support and surrounds the substrate support surface. The first ring member has a first surface roughness. The first ring member is conductive. The second ring member is located on the substrate support and surrounds the first ring member. The second ring member is insulating. At least a part of a surface of the second ring member has a second surface roughness greater than the first surface roughness. The second surface roughness is 4 to 8 μm inclusive.

[0010] In one exemplary embodiment, the first ring member contains silicon.

25 [0011] In one exemplary embodiment, the second ring member contains quartz.

[0012] In one exemplary embodiment, the second ring member includes an inner side surface facing the first ring member and an outer side surface opposite to the inner side surface, and at least the outer side surface included in the surface of the second ring member has the second surface roughness.

[0013] In one exemplary embodiment, the second ring member includes an upper surface continuous with the inner side surface and the outer side surface, and at least a part of the upper surface has the second surface roughness.

[0014] In one exemplary embodiment, the upper surface has the second surface roughness on a portion continuous with the outer side surface.

[0015] In one exemplary embodiment, the upper surface includes a first portion and a second portion. The first portion is a slope continuous with the inner side surface and extending upward. The second portion is continuous with the first portion and the outer side surface and perpendicular to the outer side surface.

[0016] In one exemplary embodiment, the second surface roughness is 5 to 7 μm inclusive.

[0017] In one exemplary embodiment, the second surface roughness is 6 μm .

[0018] In one exemplary embodiment, at least a part of the surface of the second ring member is a sandblasted surface.

[0019] In one exemplary embodiment, a ring assembly is provided. The ring assembly includes a first ring member and a second ring member. The first ring member is located on a substrate support in a chamber in a plasma processing apparatus. The substrate support includes a substrate support surface to support a substrate. The first ring member surrounds the substrate support surface. The first ring member has a first surface roughness. The first ring member is conductive. The second ring member is located on the substrate support and surrounds the first ring member. The second ring member is insulating. At least a part of a surface of the second ring member has a second surface roughness greater than the first surface roughness. The second surface roughness is 4 to 8 μm inclusive.

[0020] One or more embodiments of the present disclosure will be described below with reference to the drawings. In the drawings, like reference numerals denote the same or like components. Such components will not be described repeatedly. Unless otherwise specified, the positional relationships shown in the drawings are used to describe the vertical, lateral, and other positions. The drawings are not drawn to scale relative to the actual ratio of each component, and the actual ratio is not limited to the ratio in the drawings.

[0021] FIG. 1 is a diagram of a plasma processing system, illustrating an example structure.

In one embodiment, the plasma processing system includes a plasma processing apparatus 1 and a controller 2. The plasma processing system is an example of a substrate processing system. The plasma processing apparatus 1 is an example of a substrate processing apparatus. The plasma processing apparatus 1 includes a plasma processing chamber 10, a substrate support 11, and a plasma generator 12. The plasma processing chamber 10 has a plasma processing space. The plasma processing chamber 10 also has at least one gas inlet for supplying at least one processing gas into the plasma processing space and at least one gas outlet for exhausting the gas from the plasma processing space. The gas inlet is connected to a gas supply 20 (described later). The gas outlet is connected to an exhaust system 40 (described later). The substrate support 11 is located in the plasma processing space and has a substrate support surface for supporting a substrate.

[0022] The plasma generator 12 generates a plasma from at least one processing gas supplied into the plasma processing space. The plasma generated in the plasma processing space may be, for example, a capacitively coupled plasma (CCP), an inductively coupled plasma (ICP), an electron cyclotron resonance (ECR) plasma, a helicon wave plasma (HWP), or a surface wave plasma (SWP). The plasma generator 12 may be one of various plasma generators including an alternating current (AC) plasma generator and a direct current (DC) plasma generator. In one embodiment, an AC signal (AC power) used in the AC plasma generator has a frequency in a range of 100 kHz to 10 GHz. Thus, the AC signal may be a radio-frequency (RF) signal or a microwave signal. In one embodiment, the RF signal has a frequency in a range of 100 kHz to 150 MHz.

[0023] The controller 2 processes computer-executable instructions that cause the plasma processing apparatus 1 to perform various steps described in one or more embodiments of the present disclosure. The controller 2 may control the components of the plasma processing apparatus 1 to perform the various steps described herein. In one embodiment, some or all of the components of the controller 2 may be included in the plasma processing apparatus 1. The controller 2 may include a processor 2a1, a storage 2a2, and a communication interface 2a3. The controller 2 is implemented by, for example, a computer 2a. The processor 2a1 may perform various control operations by loading programs from the storage 2a2 and executing the

loaded programs. The program may be prestored in the storage 2a2 or may be obtained through a medium as appropriate. The obtained program is stored into the storage 2a2 to be loaded from the storage 2a2 and executed by the processor 2a1. The medium may be one of various storage media readable by the computer 2a or a communication line connected to the communication interface 2a3. The processor 2a1 may be a central processing unit (CPU). The storage 2a2 may include a random-access memory (RAM), a read-only memory (ROM), a hard disk drive (HDD), a solid-state drive (SSD), or a combination of these. The communication interface 2a3 may communicate with the plasma processing apparatus 1 through a communication line such as a local area network (LAN).

[0024] An example structure of a capacitively coupled plasma processing apparatus as an example of the plasma processing apparatus 1 will be described below. FIG. 2 is a diagram of the capacitively coupled plasma processing apparatus, illustrating an example structure.

[0025] The capacitively coupled plasma processing apparatus 1 includes a plasma processing chamber 10, a gas supply 20, a power supply 30, and the exhaust system 40. The plasma processing apparatus 1 further includes the substrate support 11 and a gas guide unit. The gas guide unit allows at least one processing gas to be introduced into the plasma processing chamber 10. The gas guide unit includes a showerhead 13. The substrate support 11 is located in the plasma processing chamber 10. The showerhead 13 is located above the substrate support 11. In one embodiment, the showerhead 13 defines at least a part of the ceiling of the plasma processing chamber 10. The plasma processing chamber 10 has a plasma processing space 10s defined by the showerhead 13, a sidewall 10a of the plasma processing chamber 10, and the substrate support 11. The plasma processing chamber 10 is grounded. The showerhead 13 and the substrate support 11 are electrically insulated from the housing of the plasma processing chamber 10.

[0026] The substrate support 11 includes a body 111 and a ring assembly 112. The body 111 includes a central portion 111a for supporting a substrate W and an annular portion 111b for supporting the ring assembly 112. A wafer is an example of the substrate W. The annular portion 111b of the body 111 surrounds the central portion 111a of the body 111 as viewed in plan. The substrate W is placeable on the central portion 111a of the body 111. The ring

assembly 112 is located on the annular portion 111b of the body 111 to surround the substrate W on the central portion 111a of the body 111. Thus, the central portion 111a is also referred to as a substrate support surface for supporting the substrate W. The annular portion 111b is also referred to as a ring support surface for supporting the ring assembly 112.

[0027] In one embodiment, the body 111 includes a base 1110 and an electrostatic chuck (ESC) 1111. The base 1110 includes a conductive member. The conductive member in the base 1110 may function as a lower electrode. The ESC 1111 is located on the base 1110. The ESC 1111 includes a ceramic member 1111a and an electrostatic electrode 1111b located inside the ceramic member 1111a. The ceramic member 1111a includes the central portion 111a.

In one embodiment, the ceramic member 1111a also includes the annular portion 111b. The annular portion 111b may be included in another member surrounding the ESC 1111, such as an annular ESC or an annular insulating member. In this case, the ring assembly 112 may be located on the annular ESC or the annular insulating member, or may be located on both the ESC 1111 and the annular insulating member. At least one RF/DC electrode coupled to an RF power supply 31 or a DC power supply 32, or both (described later) may be located inside the ceramic member 1111a. In this case, the RF/DC electrode functions as a lower electrode. When a bias RF signal or a DC signal, or both (described later) are provided to at least one RF/DC electrode, the RF/DC electrode is also referred to as a bias electrode. The conductive member in the base 1110 and at least one RF/DC electrode may function as multiple lower electrodes. The electrostatic electrode 1111b may also function as a lower electrode. The substrate support 11 thus includes at least one lower electrode.

[0028] The ring assembly 112 includes one or more annular members. In one embodiment, the one or more annular members include one or more edge rings and at least one cover ring. The edge ring(s) is formed from a conductive material or an insulating material.

The cover ring(s) is formed from an insulating material.

[0029] The substrate support 11 may include a temperature controller that adjusts the temperature of at least one of the ESC 1111, the ring assembly 112, or the substrate to a target temperature. The temperature controller may include a heater, a heat transfer medium, a channel 1110a, or a combination of these. The channel 1110a carries a heat transfer fluid such

as brine or a gas. In one embodiment, the channel 1110a is defined inside the base 1110, and one or more heaters are located inside the ceramic member 1111a in the ESC 1111. The substrate support 11 may include a heat transfer gas supply to supply a heat transfer gas into a space between the back surface of the substrate W and the central portion 111a.

5 [0030] The showerhead 13 introduces at least one processing gas from the gas supply 20 into the plasma processing space 10s. The showerhead 13 includes at least one gas inlet 13a, at least one gas-diffusion compartment 13b, and multiple gas guides 13c. The processing gas supplied to the gas inlet 13a passes through the gas-diffusion compartment 13b and is introduced into the plasma processing space 10s through the multiple gas guides 13c. The
10 showerhead 13 further includes at least one upper electrode. In addition to the showerhead 13, the gas guide unit may include one or more side gas injectors (SGIs) installed in one or more openings in the sidewall 10a.

[0031] The gas supply 20 may include at least one gas source 21 and at least one flow controller 22. In one embodiment, the gas supply 20 supplies at least one processing gas from
15 the corresponding gas source 21 to the showerhead 13 through the corresponding flow controller 22. The flow controller 22 may be, for example, a mass flow controller or a pressure-based flow controller. The gas supply 20 may further include at least one flow rate modulator that causes at least one processing gas to be supplied at a modulated flow rate or in a pulsed manner.

20 [0032] The power supply 30 includes the RF power supply 31 coupled to the plasma processing chamber 10 through at least one impedance matching circuit. The RF power supply 31 provides at least one RF signal (RF power) to at least one lower electrode or at least one upper electrode, or both. This generates a plasma from at least one processing gas supplied into the plasma processing space 10s. The RF power supply 31 may thus function as
25 at least a part of the plasma generator 12. A bias RF signal is provided to at least one lower electrode to generate a bias potential in the substrate W, thus drawing ion components in the generated plasma toward the substrate W.

[0033] In one embodiment, the RF power supply 31 includes a first RF generator 31a and a second RF generator 31b. The first RF generator 31a is coupled to at least one lower

electrode or at least one upper electrode, or both through at least one impedance matching circuit to generate a source RF signal (source RF power) for plasma generation. In one embodiment, the source RF signal has a frequency in a range of 10 to 150 MHz. In one embodiment, the first RF generator 31a may generate multiple source RF signals with different frequencies. The one or more generated source RF signals are provided to at least one lower electrode or at least one upper electrode, or both.

[0034] The second RF generator 31b is coupled to at least one lower electrode through at least one impedance matching circuit to generate a bias RF signal (bias RF power). The frequency of the bias RF signal may be the same as or different from the frequency of the source RF signal. In one embodiment, the bias RF signal has a lower frequency than the source RF signal. In one embodiment, the bias RF signal has a frequency in a range of 100 kHz to 60 MHz. In one embodiment, the second RF generator 31b may generate multiple bias RF signals with different frequencies. The one or more generated bias RF signals are provided to at least one lower electrode. In various embodiments, at least one of the source RF signal or the bias RF signal may be pulsed.

[0035] The power supply 30 may include the DC power supply 32 coupled to the plasma processing chamber 10. The DC power supply 32 includes a first DC generator 32a and a second DC generator 32b. In one embodiment, the first DC generator 32a is coupled to at least one lower electrode to generate a first DC signal. The generated first DC signal is applied to at least one lower electrode. In one embodiment, the second DC generator 32b is coupled to at least one upper electrode to generate a second DC signal. The generated second DC signal is applied to at least one upper electrode.

[0036] In various embodiments, the first DC signal and the second DC signal may be pulsed. In this case, a sequence of voltage pulses is applied to at least one lower electrode or at least one upper electrode, or both. The voltage pulses may have rectangular, trapezoidal, or triangular pulse waveforms, or a combination of these. In one embodiment, a waveform generator for generating a sequence of voltage pulses based on DC signals is coupled between the first DC generator 32a and at least one lower electrode. Thus, the first DC generator 32a and the waveform generator form a voltage pulse generator. When the second DC generator

32b and the waveform generator form a voltage pulse generator, the voltage pulse generator is coupled to at least one upper electrode. The voltage pulses may have positive polarity or negative polarity. The sequence of voltage pulses may include one or more positive voltage pulses and one or more negative voltage pulses within one cycle. The power supply 30 may include the first DC generator 32a and the second DC generator 32b in addition to the RF power supply 31 or may include the first DC generator 32a in place of the second RF generator 31b.

[0037] The exhaust system 40 is connectable to, for example, a gas outlet 10e in the bottom of the plasma processing chamber 10. The exhaust system 40 may include a pressure control valve and a vacuum pump. The pressure control valve regulates the pressure in the plasma processing space 10s. The vacuum pump may be a turbomolecular pump, a dry pump, or a combination of these.

[0038] FIG. 3 is an enlarged partial view of the ring assembly 112 in an example structure. FIG. 3 also shows a part of the substrate W and a part of the substrate support 11 in an example structure. The ring assembly 112 may include an edge ring 113 and a cover ring 114. The edge ring 113 is an example of the first ring member. The cover ring 114 is an example of the second ring member.

[0039] The edge ring 113 may be located on the substrate support 11 and surround the substrate support surface (central portion 111a). In one embodiment, the substrate support surface is circular as viewed in plan, and the edge ring 113 is a ring as viewed in plan. The edge ring 113 may contain a material that is conductive. In one embodiment, the edge ring 113 is made of a material containing silicon. In one example, the edge ring 113 may be made of silicon (Si) or silicon carbide (SiC). The edge ring 113 has a surface roughness Ra1. The surface roughness Ra1 is an example of the first surface roughness. In one embodiment, the edge ring 113 may have a surface roughness Ra1 of 0.2 to 0.8 μm .

[0040] The cover ring 114 may be located on the substrate support 11 and surround the edge ring 113. In one embodiment, the cover ring 114 may cover a part of a side surface of the substrate support 11. In one embodiment, the cover ring 114 is a ring as viewed in plan. The cover ring 114 may include an inner side surface 114a, an outer side surface 114b, and an upper surface 114c.

[0041] The inner side surface 114a may face the edge ring 113. The inner side surface 114a may be substantially perpendicular to the substrate support surface of the substrate support 11. The outer side surface 114b of the cover ring 114 may be a surface opposite to the inner side surface 114a. In other words, the inner side surface 114a and the outer side surface 114b may be concentric with each other about the center of the substrate support surface as viewed in plan.

[0042] The upper surface 114c may include a first portion 114c-1 and a second portion 114c-2. The first portion 114c-1 may be continuous with the inner side surface 114a. The first portion 114c-1 may be a slope. In other words, the first portion 114c-1 may be higher at positions from the inner side surface 114a to the second portion 114c-2. The second portion 114c-2 may be substantially perpendicular to the outer side surface 114b. In other words, the second portion 114c-2 may be parallel to the substrate support surface.

[0043] The cover ring 114 may contain a material that is insulating. In one example, the cover ring 114 may contain quartz. The cover ring 114 has a surface roughness Ra2 on at least a part of the cover ring 114. The surface roughness Ra2 is an example of the second surface roughness. In one example, the cover ring 114 may have the surface roughness Ra2 on at least a part of the outer side surface 114b and on at least a part of the second portion 114c-2 of the upper surface 114c. At least a part of the second portion 114c-2 may be a part of the second portion 114c-2 that is continuous with the outer side surface 114b. In one embodiment, the cover ring 114 may have the surface roughness Ra2 across the upper surface 114c and the outer side surface 114b.

[0044] The surface roughness Ra2 is different from the surface roughness Ra1. The surface roughness Ra2 may be greater than the surface roughness Ra1. In one example, the surface roughness Ra2 may be 4 to 8 μm , 5 to 7 μm , or about 6 μm . The surface of the cover ring 114 with the surface roughness Ra2 may be formed by, for example, sandblasting. In one example, a portion of the surface of the cover ring 114 exposed in a space in the plasma processing chamber 10 or a part of the portion may be sandblasted.

[0045] FIG. 4 is a flowchart of an example plasma processing method. The plasma processing method shown in FIG. 4 (hereafter also referred to as the method) may be, for

example, plasma processing including etching of a substrate. The method includes a step of placing a ring assembly (ST1), a step of providing a substrate (ST2), and a step of generating a plasma (ST3). The method may be implemented by the plasma processing system or the plasma processing apparatus illustrated in FIGs. 1 and 2. The ring assembly may be placed manually by an operator in step ST1.

[0046] In step ST1, the ring assembly 112 is placed. The edge ring 113 is placed to surround the substrate processing surface on the substrate support 11. The cover ring 114 is placed to surround the edge ring 113. After the ring assembly 112 is placed, the pressure in the plasma processing chamber 10 may be reduced.

[0047] In step ST2, the substrate W is provided. Providing the substrate W includes placing the substrate W on the substrate support surface. In one example, the substrate W includes an etching target film and a mask on the etching target film.

[0048] A plasma is then generated in the plasma processing chamber 10 in step ST3. In step ST3, a processing gas is first supplied into the plasma processing chamber 10. The processing gas may be selected as appropriate based on the etching target film or the mask, or both, included in the substrate W. A source RF signal is then provided to the upper electrode or the lower electrode. This generates a plasma from the processing gas in the plasma processing chamber 10. In step ST3, a bias signal may be provided to the lower electrode.

[0049] In one embodiment of the present disclosure, the cover ring 114 has a surface roughness Ra2 of 4 to 8 μm inclusive. Thus, a product or a byproduct, or both, adhering to the cover ring 114 during plasma processing are less likely to separate from the cover ring 114. This can also reduce particle generation in plasma processing. The cover ring 114 with a surface roughness Ra2 of 5 to 7 μm inclusive can further reduce or prevent the separation.

[0050] One or more embodiments of the present disclosure may include, for example, the structures described below.

Aspect 1

[0051] A plasma processing apparatus, comprising:

a chamber;

a substrate support in the chamber, the substrate support including a substrate support

surface to support a substrate;

a first ring member located on the substrate support and surrounding the substrate support surface, the first ring member having a first surface roughness, the first ring member being conductive; and

- 5 a second ring member located on the substrate support and surrounding the first ring member, the second ring member being insulating, at least a part of a surface of the second ring member having a second surface roughness greater than the first surface roughness, the second surface roughness being 4 to 8 μm inclusive.

Aspect 2

- 10 [0052] The plasma processing apparatus according to aspect 1, wherein
the first ring member contains silicon.

Aspect 3

- [0053] The plasma processing apparatus according to aspect 1 or aspect 2, wherein
the second ring member contains quartz.

15 Aspect 4

- [0054] The plasma processing apparatus according to any one of aspects 1 to 3, wherein
the second ring member includes an inner side surface facing the first ring member and an
outer side surface opposite to the inner side surface, and
at least the outer side surface included in the surface of the second ring member has the
20 second surface roughness.

Aspect 5

- [0055] The plasma processing apparatus according to aspect 4, wherein
the second ring member includes an upper surface continuous with the inner side surface
and the outer side surface, and at least a part of the upper surface has the second surface
25 roughness.

Aspect 6

- [0056] The plasma processing apparatus according to aspect 5, wherein
the upper surface has the second surface roughness on a portion continuous with the outer
side surface.

Aspect 7

[0057] The plasma processing apparatus according to aspect 6, wherein

the upper surface includes a first portion and a second portion, the first portion is a slope continuous with the inner side surface and extending upward, and the second portion is continuous with the first portion and the outer side surface and perpendicular to the outer side surface.

Aspect 8

[0058] The plasma processing apparatus according to any one of aspects 1 to 7, wherein the second surface roughness is 5 to 7 μm inclusive.

10 Aspect 9

[0059] The plasma processing apparatus according to aspect 8, wherein the second surface roughness is 6 μm .

Aspect 10

[0060] The plasma processing apparatus according to any one of aspects 1 to 9, wherein at least a part of the surface of the second ring member is a sandblasted surface.

Aspect 11

A ring assembly, comprising:

a first ring member located on a substrate support in a chamber in a plasma processing apparatus, the substrate support including a substrate support surface to support a substrate, the first ring member surrounding the substrate support surface, the first ring member having a first surface roughness, the first ring member being conductive; and

a second ring member located on the substrate support and surrounding the first ring member, the second ring member being insulating, at least a part of a surface of the second ring member having a second surface roughness greater than the first surface roughness, the second surface roughness being 4 to 8 μm inclusive.

[0061] The exemplary embodiments described above may be modified variously without departing from the scope and spirit of the present disclosure. For example, some components in one embodiment may be added to other embodiments within the ordinary level of creativity of those skilled in the art. In some embodiments, some of the components may be replaced

with the corresponding components in other embodiments.

REFERENCE SIGNS LIST

[0062]

- 5 1 Plasma processing apparatus
- 11 Substrate support
- 112 Ring assembly
- 113 Edge ring
- 114 Cover ring
- 10 114a Inner side surface
- 114b Outer side surface
- 114c Upper surface
- 114c-1 First portion
- 114c-2 Second portion
- 15 W Substrate

CLAIMS

1. A plasma processing apparatus, comprising:

a chamber;

a substrate support in the chamber, the substrate support including a substrate support

5 surface to support a substrate;

a first ring member located on the substrate support and surrounding the substrate support surface, the first ring member having a first surface roughness, the first ring member being conductive; and

a second ring member located on the substrate support and surrounding the first ring
10 member, the second ring member being insulating, at least a part of a surface of the second ring member having a second surface roughness greater than the first surface roughness, the second surface roughness being 4 to 8 μm inclusive.

2. The plasma processing apparatus according to claim 1, wherein
the first ring member contains silicon.

15 3. The plasma processing apparatus according to claim 2, wherein
the second ring member contains quartz.

4. The plasma processing apparatus according to claim 1, wherein
the second ring member includes an inner side surface facing the first ring member and an
outer side surface opposite to the inner side surface, and

at least the outer side surface included in the surface of the second ring member has the second surface roughness.

5. The plasma processing apparatus according to claim 4, wherein

the second ring member includes an upper surface continuous with the inner side surface

5 and the outer side surface, and at least a part of the upper surface has the second surface roughness.

6. The plasma processing apparatus according to claim 5, wherein

the upper surface has the second surface roughness on a portion continuous with the outer side surface.

10 7. The plasma processing apparatus according to claim 6, wherein

the upper surface includes a first portion and a second portion, the first portion is a slope continuous with the inner side surface and extending upward, and the second portion is continuous with the first portion and the outer side surface and perpendicular to the outer side surface.

15 8. The plasma processing apparatus according to any one of claims 1 to 7, wherein

the second surface roughness is 5 to 7 μm inclusive.

9. The plasma processing apparatus according to claim 8, wherein

the second surface roughness is 6 μm .

10. The plasma processing apparatus according to claim 1, wherein

at least a part of the surface of the second ring member is a sandblasted surface.

11. A ring assembly, comprising:

a first ring member located on a substrate support in a chamber in a plasma processing apparatus, the substrate support including a substrate support surface to support a substrate, the

5 first ring member surrounding the substrate support surface, the first ring member having a first surface roughness, the first ring member being conductive; and

a second ring member located on the substrate support and surrounding the first ring member, the second ring member being insulating, at least a part of a surface of the second ring member having a second surface roughness greater than the first surface roughness, the second

10 surface roughness being 4 to 8 μm inclusive.