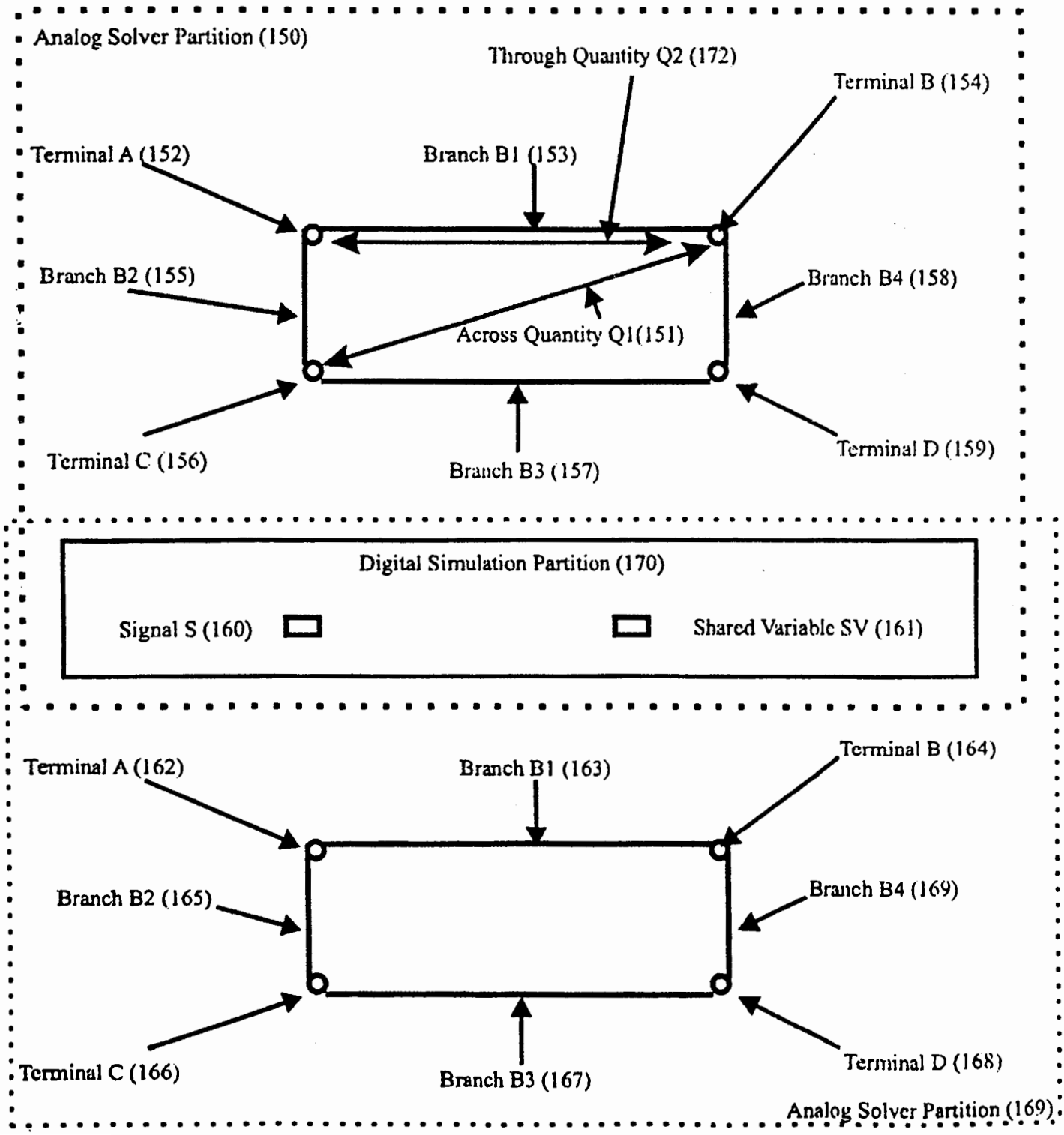
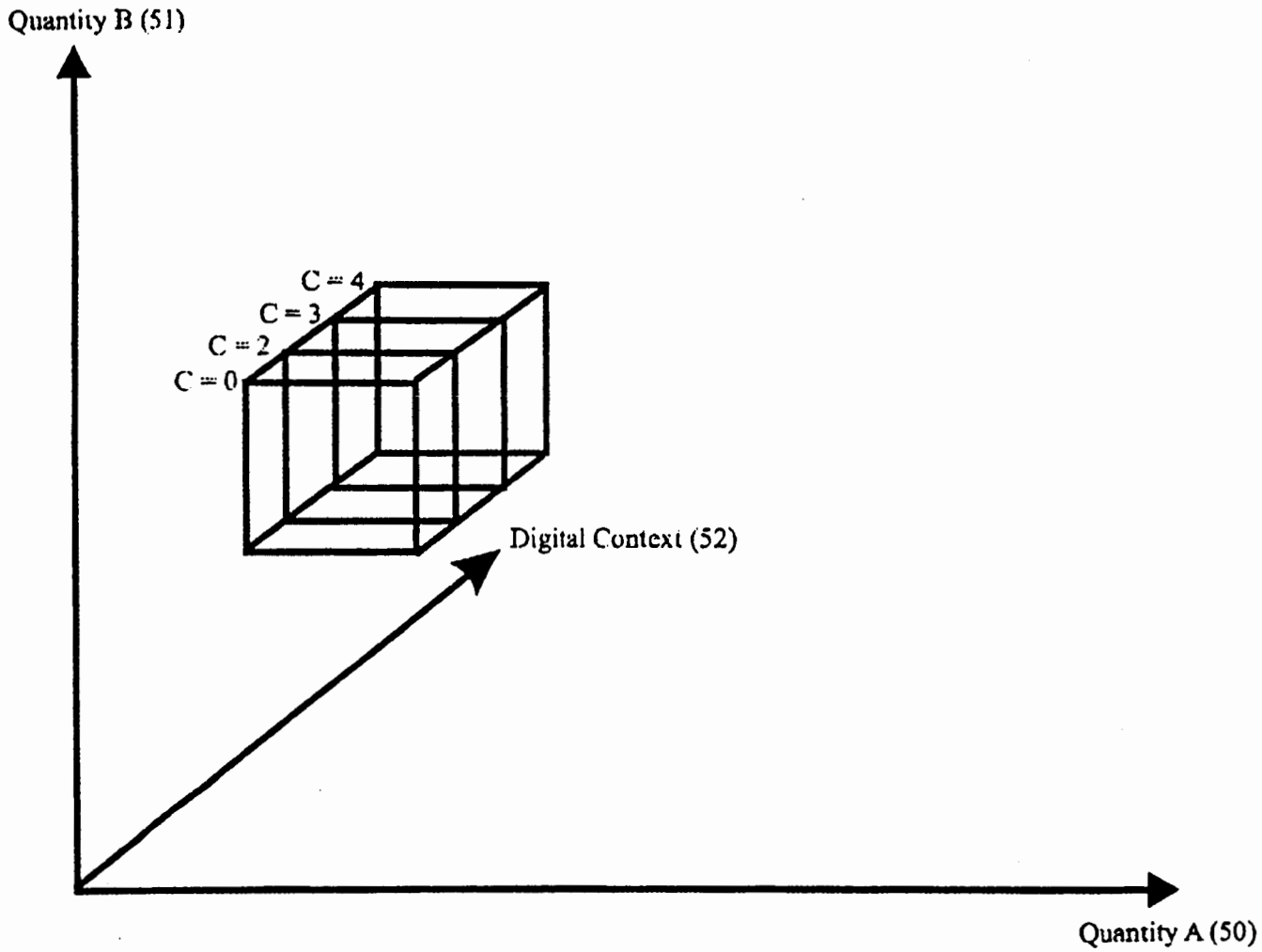
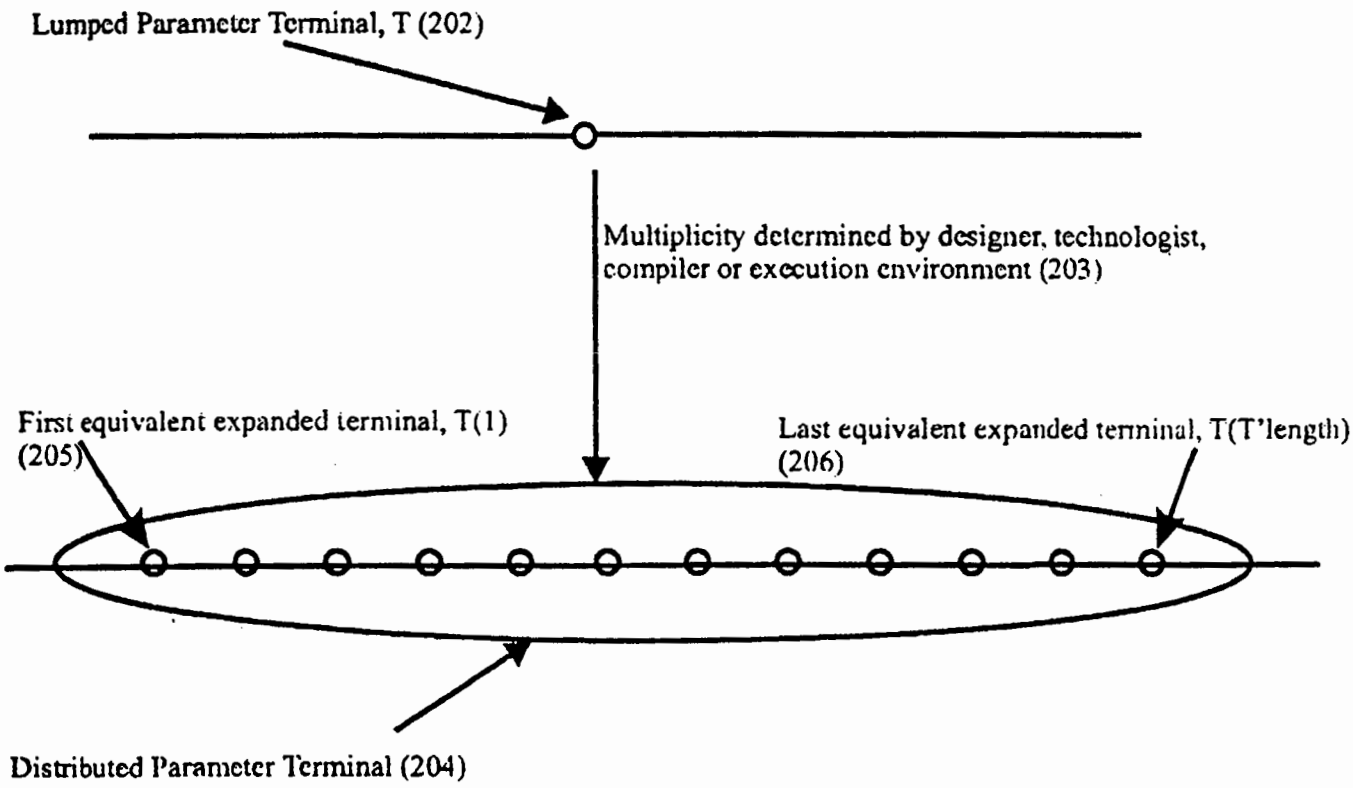
Drawing 1


Analog Solver Partition (150)
Through Quantity Q2 (172)
Terminal B (154)
Terminal A (152)
Branch B1 (153)
Branch B2 (155)
Branch B4 (158)
Across Quantity Q1(151)
Terminal C (156)
Branch B3 (157)
Terminal D (159)
Digital Simulation Partition (170)
Signal S (160)
Shared Variable SV (161)
Terminal A (162)
Branch B1 (163)
Terminal B (164)
Branch B2 (165)
Branch B4 (169)
Terminal C (166)
Branch B3 (167)
Terminal D (168)
Analog Solver Partition (169)

Drawing 2



Drawing 3

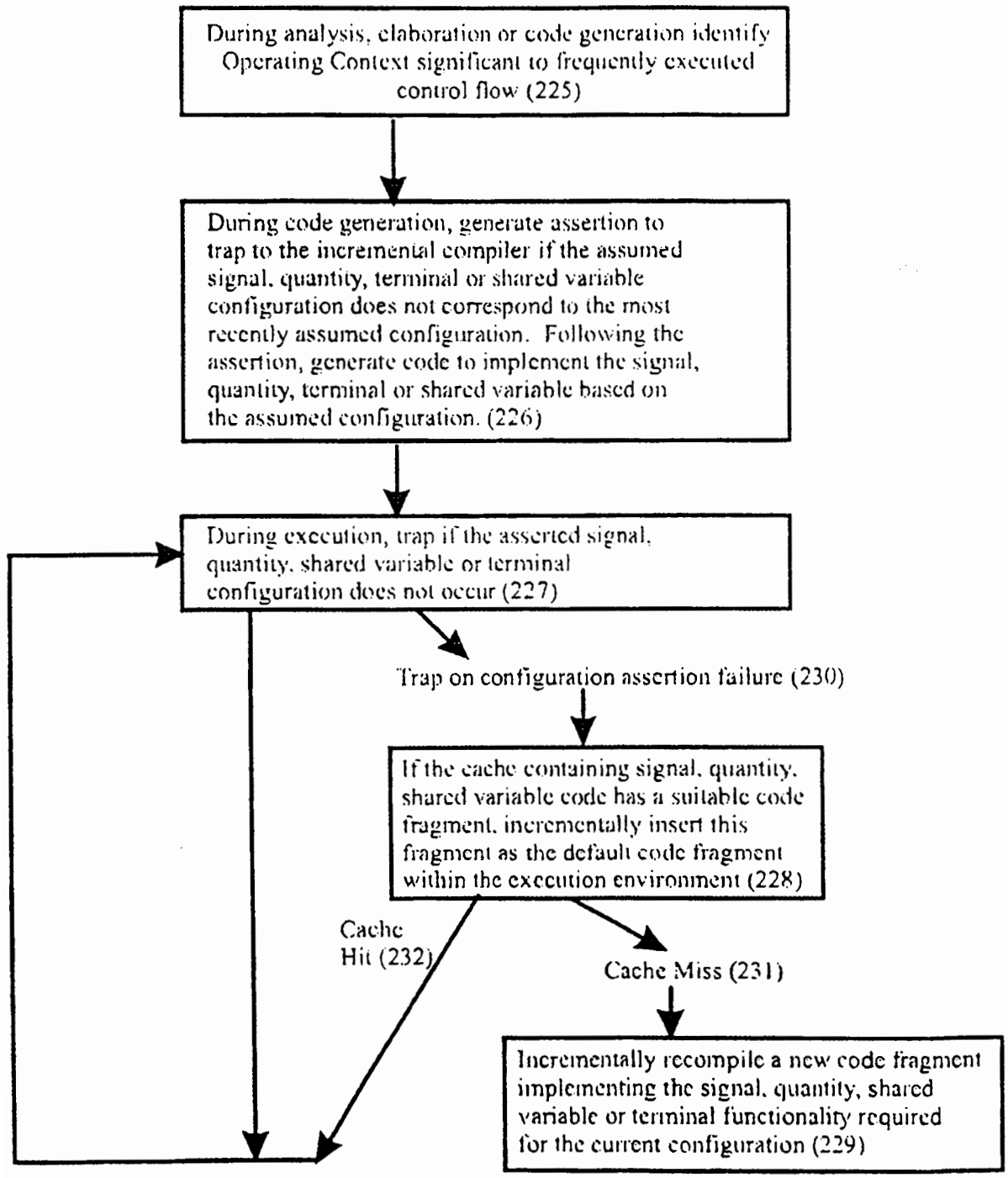

Lumped Parameter Terminal, T (202)
Multiplicity determined by designer, technologist, compiler or execution environment (203)
First equivalent expanded terminal, T(1) (205)
Last equivalent expanded terminal, T(T'length) (206)
Distributed Parameter Terminal (204)

Drawing 4

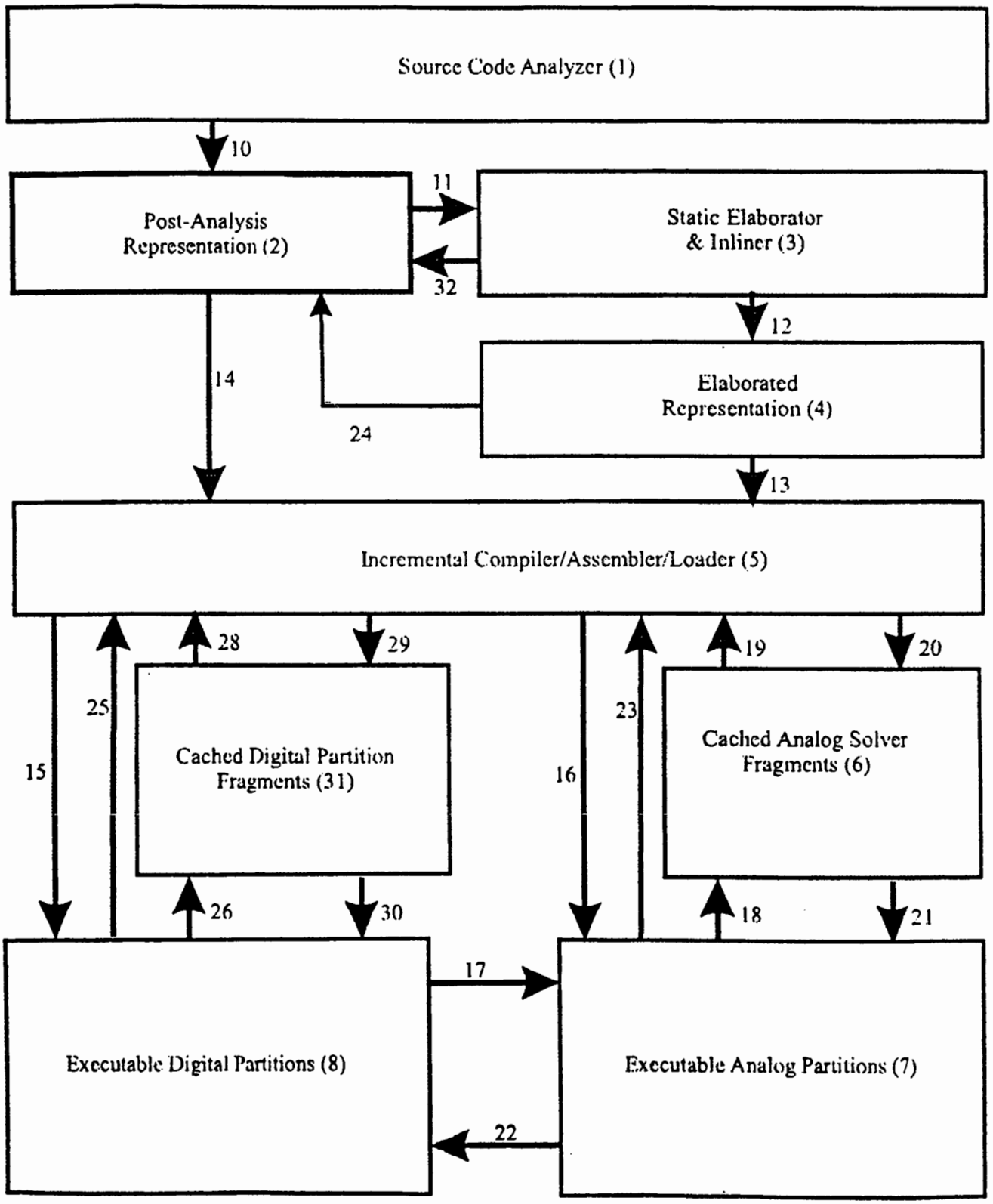
```
(210) subtype voltage is real;
(211) subtype current is real;
(212) nature tap is voltage across current;
(213) nature taps is array <> of tap;
(214) procedure transmission_line (t: taps) is
(215)     begin
(216)         -- VHDL RF/MW implementation of transmission line
(217)     end procedure transmission_line;
(218) subnature trace is transmission_line taps;
(219) terminal board_trace: trace;
```

Extract from example of VHDL-RF/MW model source code(201)

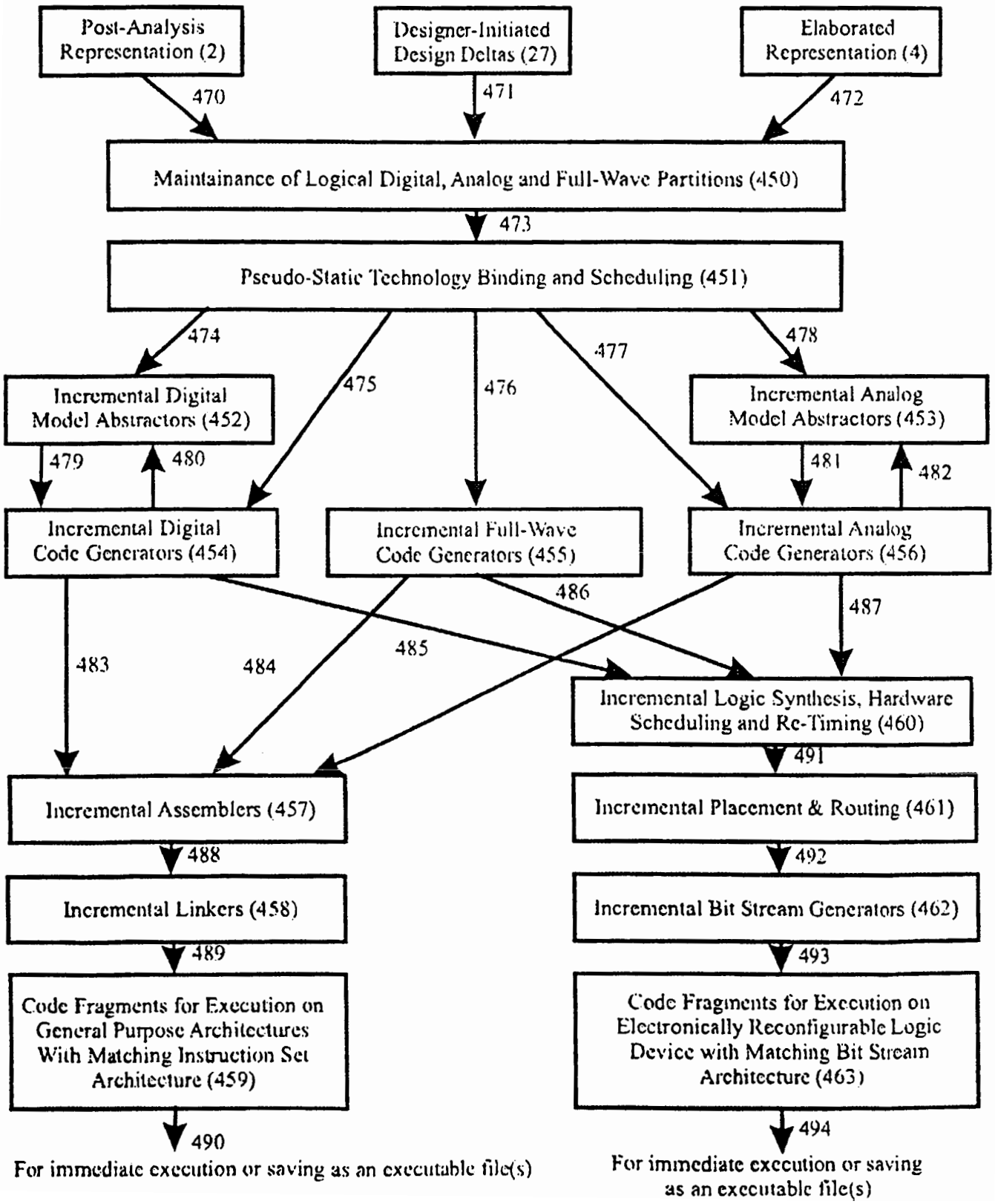
Drawing 5


During analysis, elaboration or code generation identify Operating Context significant to frequently executed control flow (225)
During code generation, generate assertion to trap to the incremental compiler if the assumed signal, quantity, terminal or shared variable configuration does not correspond to the most recently assumed configuration. Following the assertion, generate code to implement the signal, quantity, terminal or shared variable based on the assumed configuration. (226)
During execution, trap if the asserted signal, quantity, shared variable or terminal configuration does not occur (227)
Trap on configuration assertion failure (230)
If the cache containing signal, quantity, shared variable code has a suitable code fragment, incrementally insert this fragment as the default code fragment within the execution environment (228)
Cache Hit (232)
Cache Miss (231)
Incrementally recompile a new code fragment implementing the signal, quantity, shared variable or terminal functionality required for the current configuration (229)

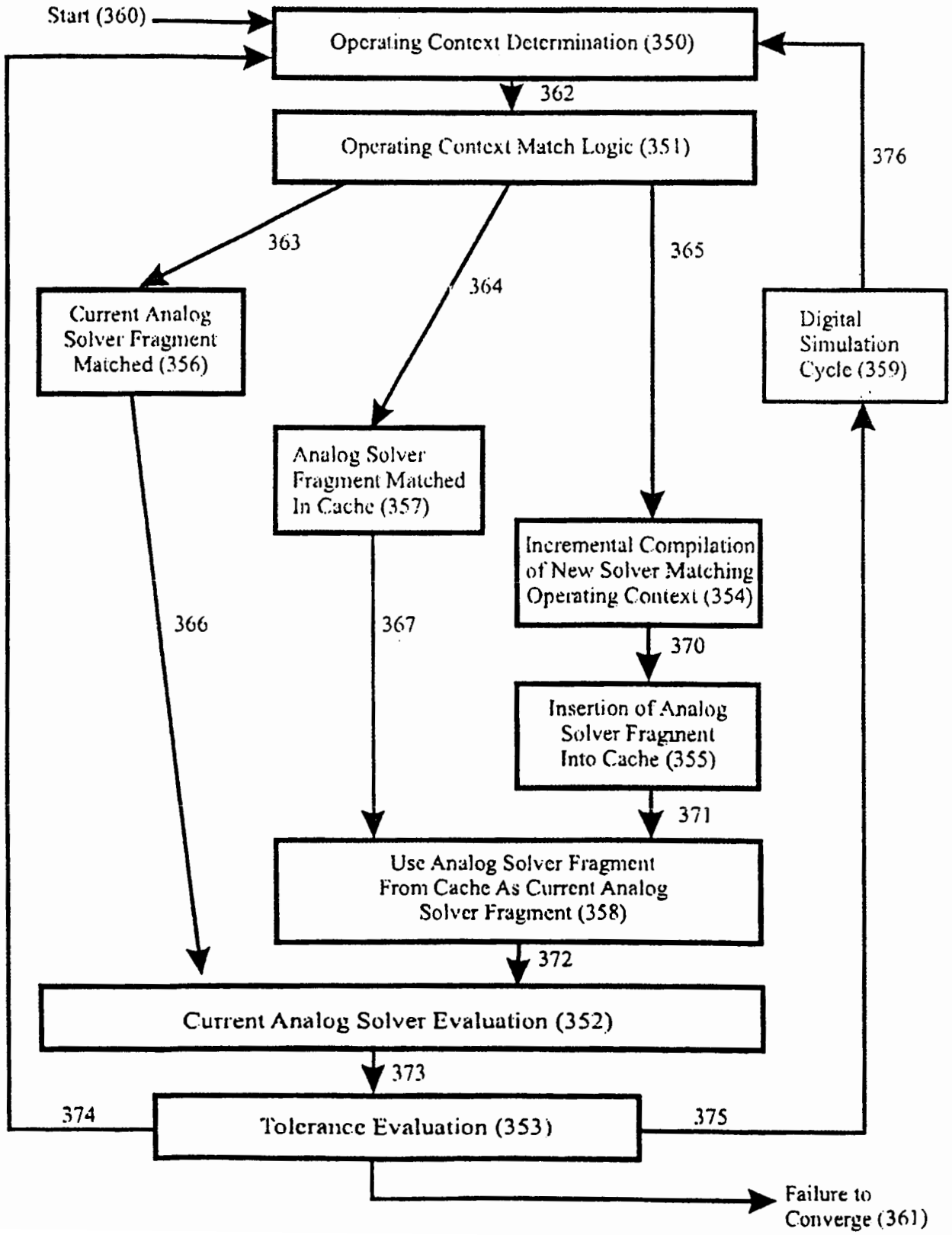
Drawing 6


Source Code Analyzer (1)
10
Post-Analysis Representation (2)
11
Static Elaborator & Inliner (3)
32
12
14
Elaborated Representation (4)
24
13
Incremental Compiler/Assembler/Loader (5)
28
29
19
20
25
23
Cached Digital Partition Fragments (31)
Cached Analog Solver Fragments (6)
15
16
26
30
18
21
17
Executable Digital Partitions (8)
Executable Analog Partitions (7)
22

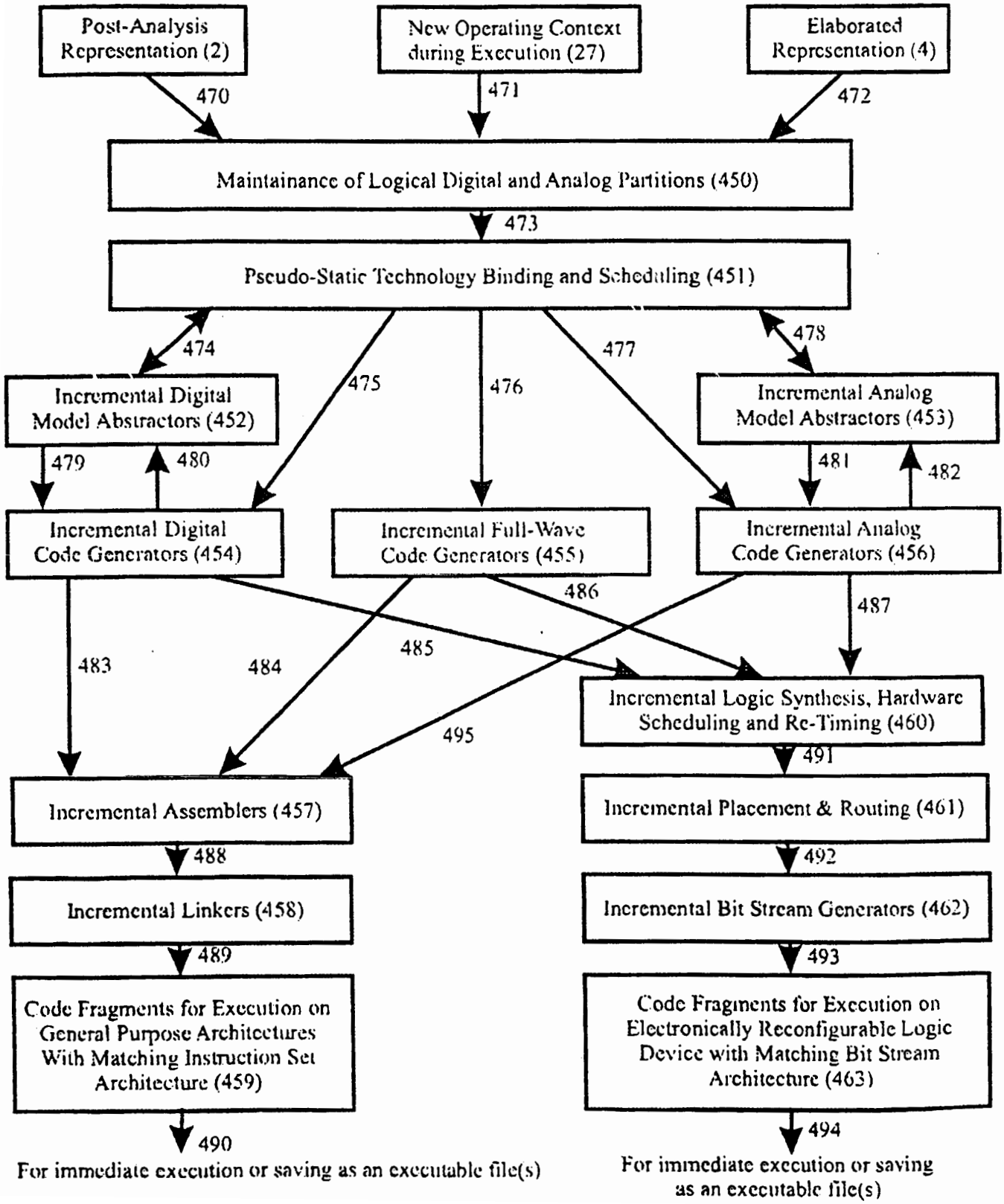
Drawing 7


Post-Analysis Representation (2)
Designer-Initiated Design Deltas (27)
Elaborated Representation (4)
470
471
472
Maintainance of Logical Digital, Analog and Full-Wave Partitions (450)
473
Pseudo-Static Technology Binding and Scheduling (451)
474
475
476
477
478
Incremental Digital Model Abstractors (452)
Incremental Analog Model Abstractors (453)
479
480
481
482
Incremental Digital Code Generators (454)
Incremental Full-Wave Code Generators (455)
Incremental Analog Code Generators (456)
483
484
485
486
487
Incremental Logic Synthesis, Hardware Scheduling and Re-Timing (460)
491
Incremental Assemblers (457)
Incremental Placement & Routing (461)
488
492
Incremental Linkers (458)
Incremental Bit Stream Generators (462)
489
493
Code Fragments for Execution on General Purpose Architectures With Matching Instruction Set Architecture (459)
Code Fragments for Execution on Electronically Reconfigurable Logic Device with Matching Bit Stream Architecture (463)
490
494
For immediate execution or saving as an executable file(s)
For immediate execution or saving as an executable file(s)

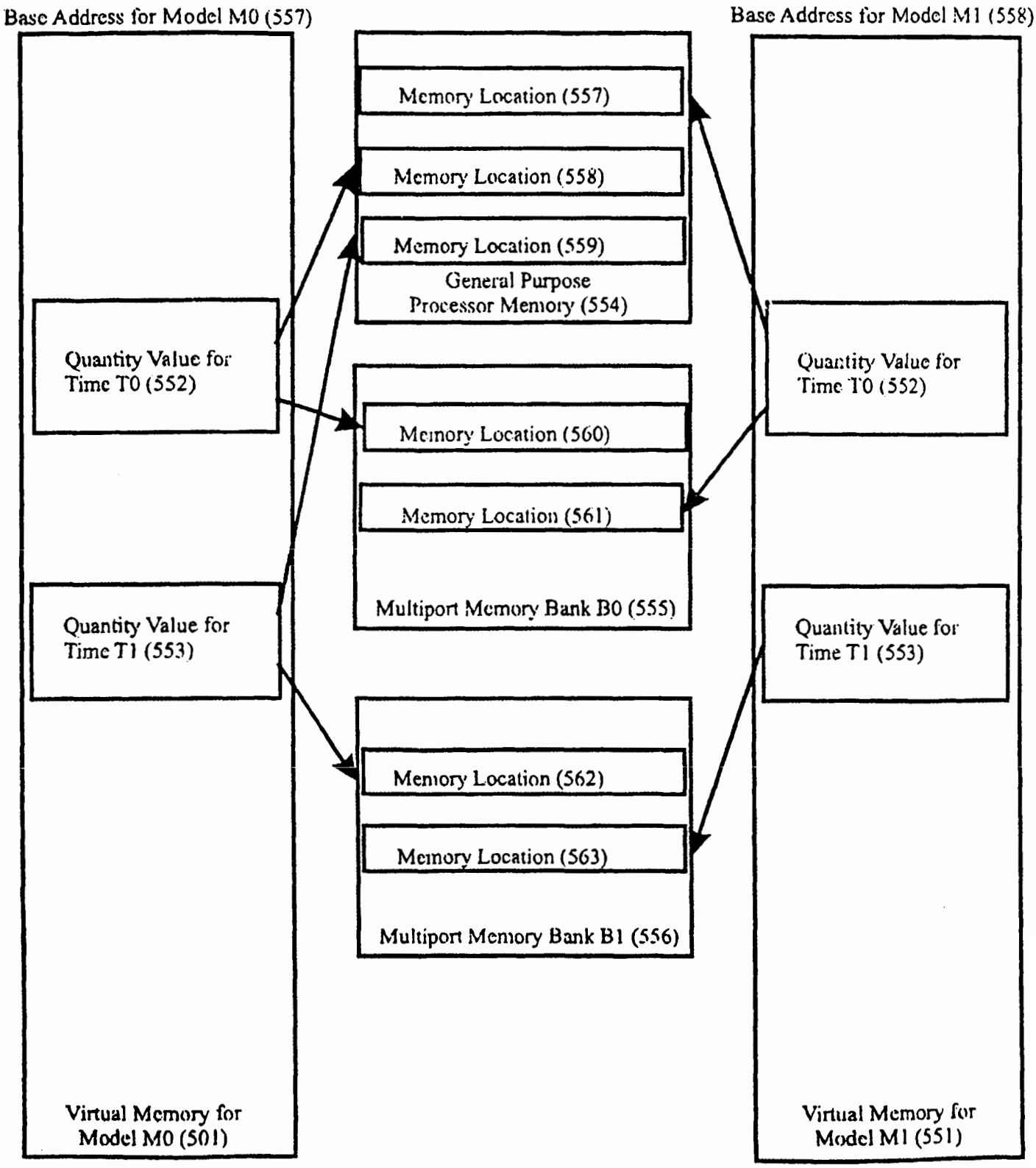
Drawing 8


Start (360)
Operating Context Determination (350)
362
Operating Context Match Logic (351)
376
363
364
365
Current Analog Solver Fragment Matched (356)
Digital Simulation Cycle (359)
Analog Solver Fragment Matched In Cache (357)
Incremental Compilation of New Solver Matching Operating Context (354)
366
367
370
Insertion of Analog Solver Fragment Into Cache (355)
371
Use Analog Solver Fragment From Cache As Current Analog Solver Fragment (358)
372
Current Analog Solver Evaluation (352)
373
374
Tolerance Evaluation (353)
375
Failure to Converge (361)

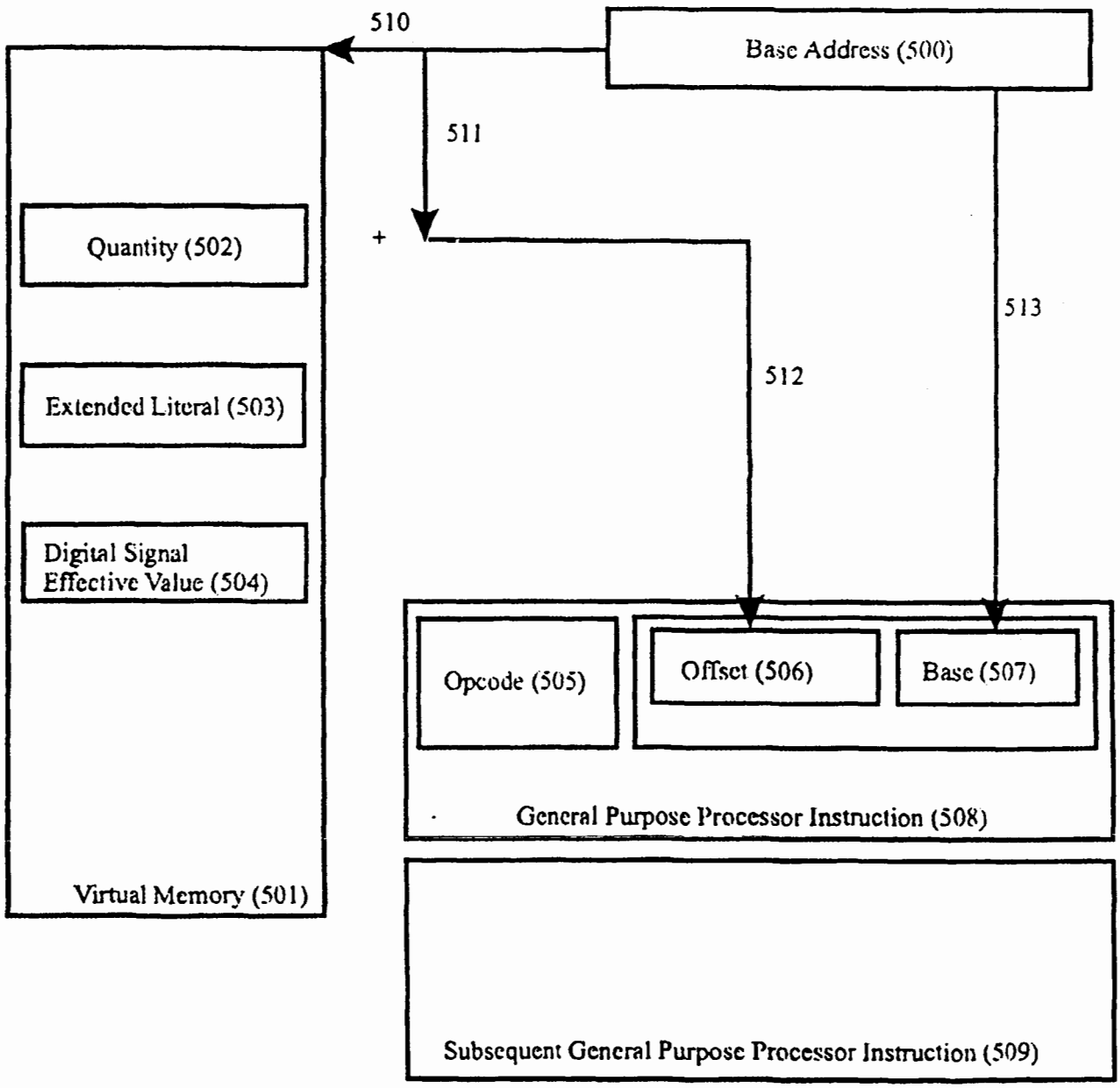
Drawing 9


Post-Analysis Representation (2)
New Operating Context during Execution (27)
Elaborated Representation (4)
470
471
472
Maintainance of Logical Digital and Analog Partitions (450)
473
Pseudo-Static Technology Binding and Scheduling (451)
474
475
476
477
478
Incremental Digital Model Abstractors (452)
Incremental Analog Model Abstractors (453)
479
480
481
482
Incremental Digital Code Generators (454)
Incremental Full-Wave Code Generators (455)
Incremental Analog Code Generators (456)
483
484
485
486
487
Incremental Logic Synthesis, Hardware Scheduling and Re-Timing (460)
491
495
Incremental Assemblers (457)
Incremental Placement & Routing (461)
488
492
Incremental Linkers (458)
Incremental Bit Stream Generators (462)
489
493
Code Fragments for Execution on General Purpose Architectures With Matching Instruction Set Architecture (459)
Code Fragments for Execution on Electronically Reconfigurable Logic Device with Matching Bit Stream Architecture (463)
490
494
For immediate execution or saving as an executable file(s)
For immediate execution or saving as an executable file(s)

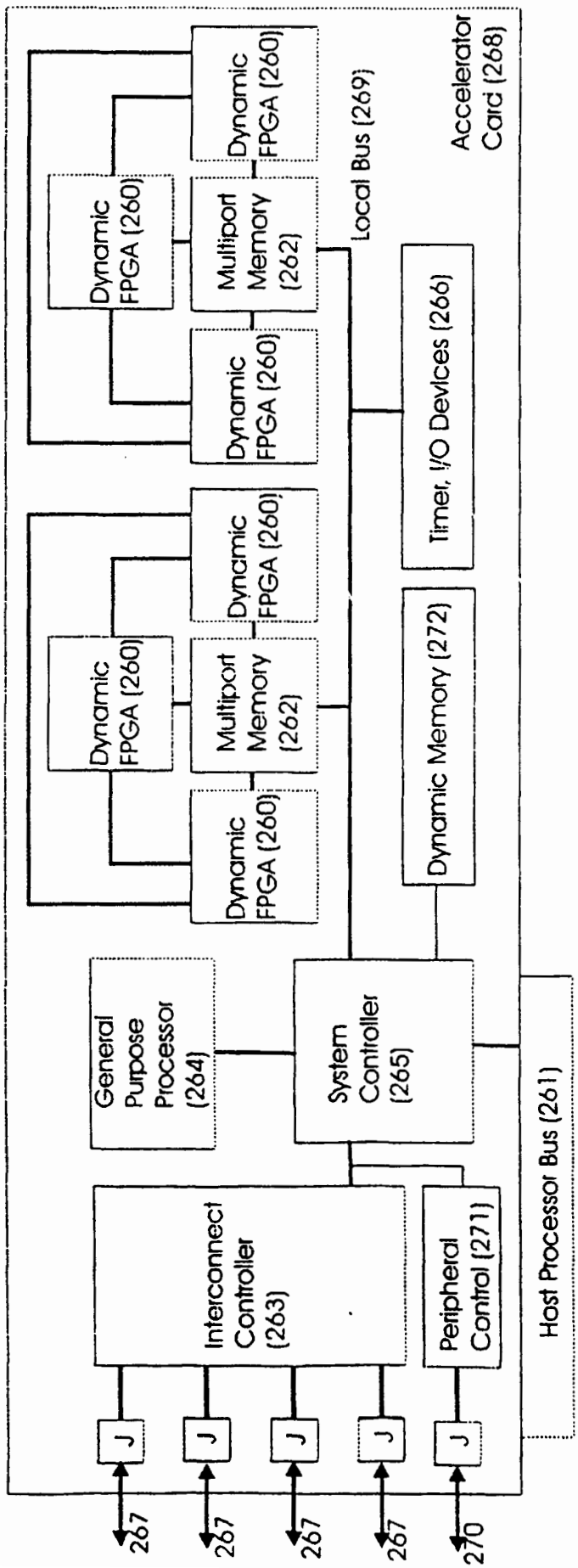
Drawing 10


Base Address for Model M0 (557)
Base Address for Model M1 (558)
Memory Location (557)
Memory Location (558)
Memory Location (559)
General Purpose Processor Memory (554)
Quantity Value for Time T0 (552)
Memory Location (560)
Memory Location (561)
Multiport Memory Bank B0 (555)
Quantity Value for Time T1 (553)
Memory Location (562)
Memory Location (563)
Multiport Memory Bank B1 (556)
Quantity Value for Time T0 (552)
Quantity Value for Time T1 (553)
Virtual Memory for Model M0 (501)
Virtual Memory for Model M1 (551)

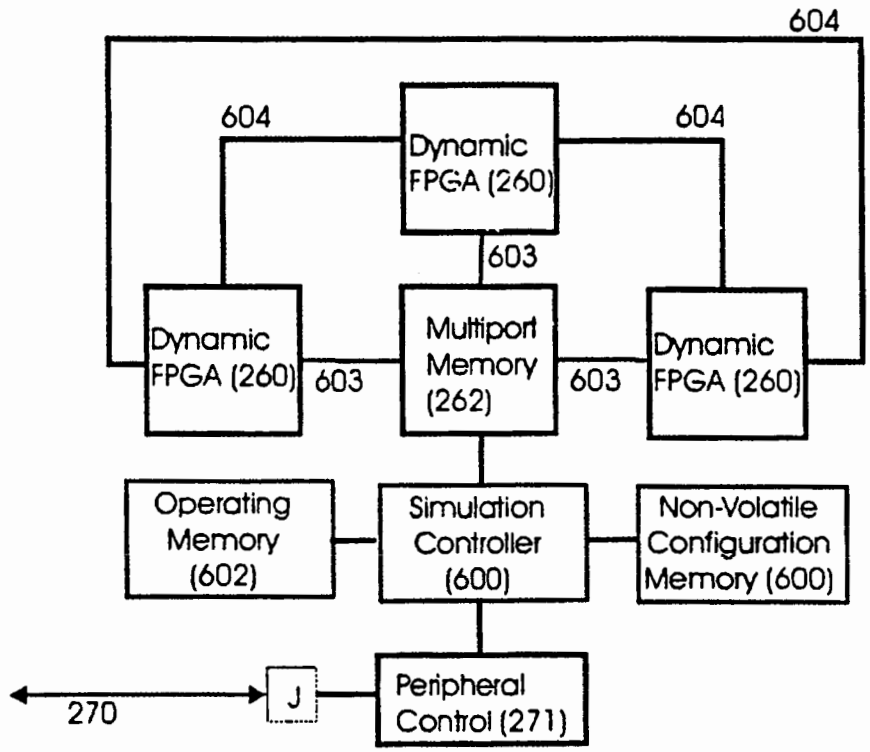
Drawing 11


510
Base Address (500)
511
+
Quantity (502)
513
512
Extended Literal (503)
Digital Signal
Effective Value (504)
Opcode (505)
Offset (506)
Base (507)
General Purpose Processor Instruction (508)
Virtual Memory (501)
Subsequent General Purpose Processor Instruction (509)

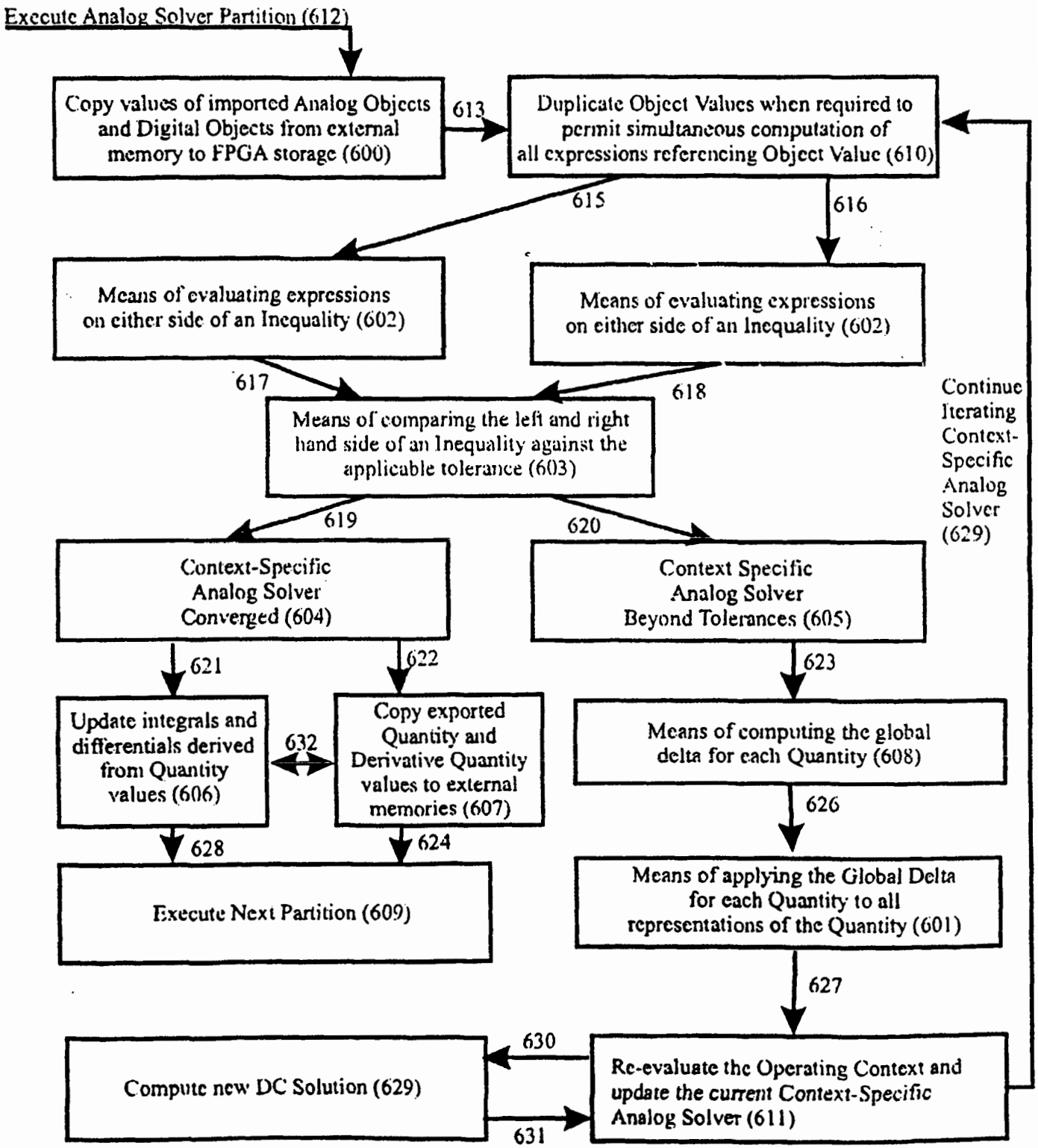
Drawing 12


Accelerator Card (268)
Local Bus (269)
Dynamic FPGA (260)
Multiport Memory (262)
Timer, I/O Devices (266)
Dynamic Memory (272)
General Purpose Processor (264)
System Controller (265)
Interconnect Controller (263)
Peripheral Control (271)
Host Processor Bus (261)
J
267
270

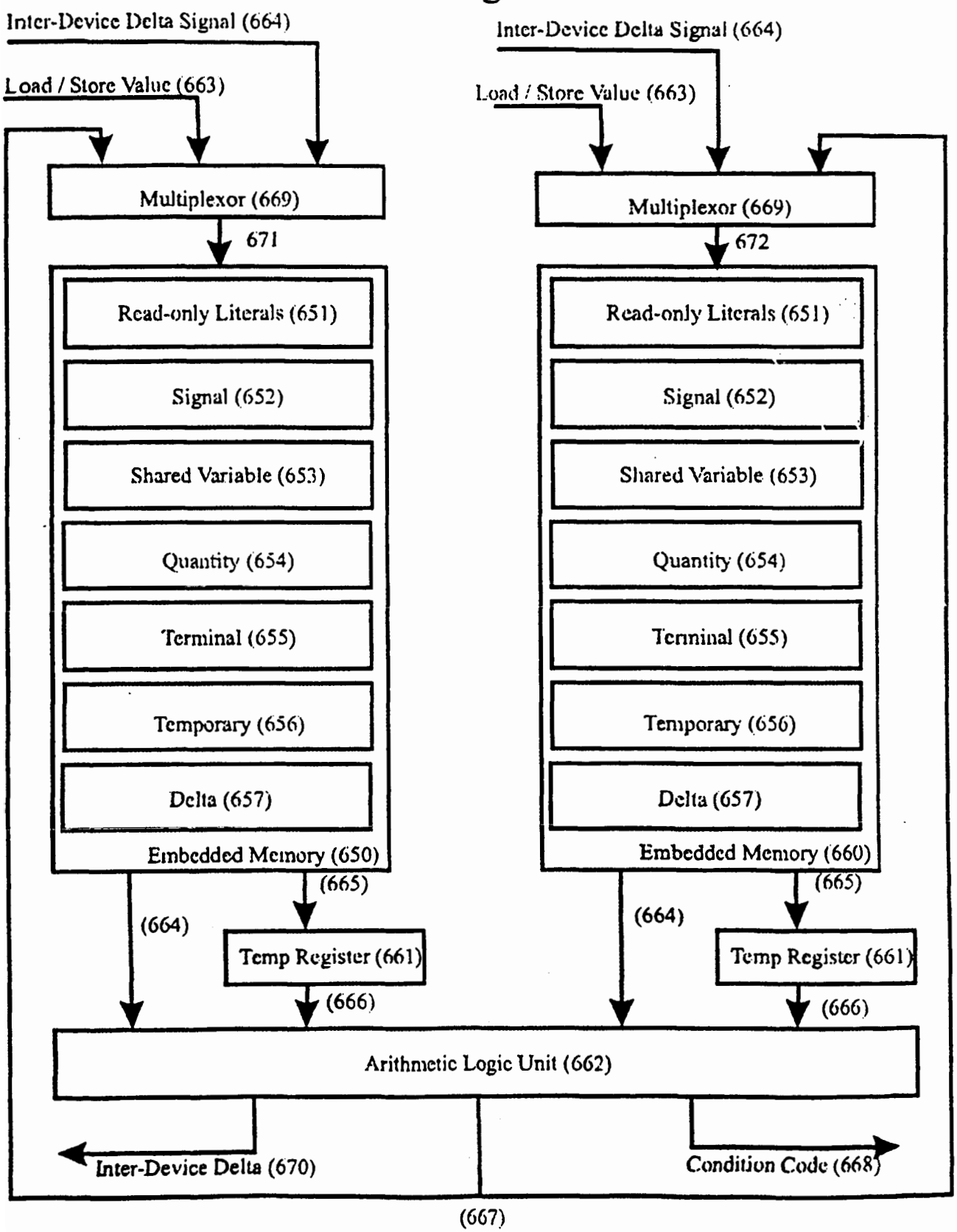
Drawing 13


604
604
Dynamic FPGA (260)
604
603
Dynamic FPGA (260)
603
Multiport Memory (262)
603
Dynamic FPGA (260)
Operating Memory (602)
Simulation Controller (600)
Non-Volatile Configuration Memory (600)
270
J
Peripheral Control (271)

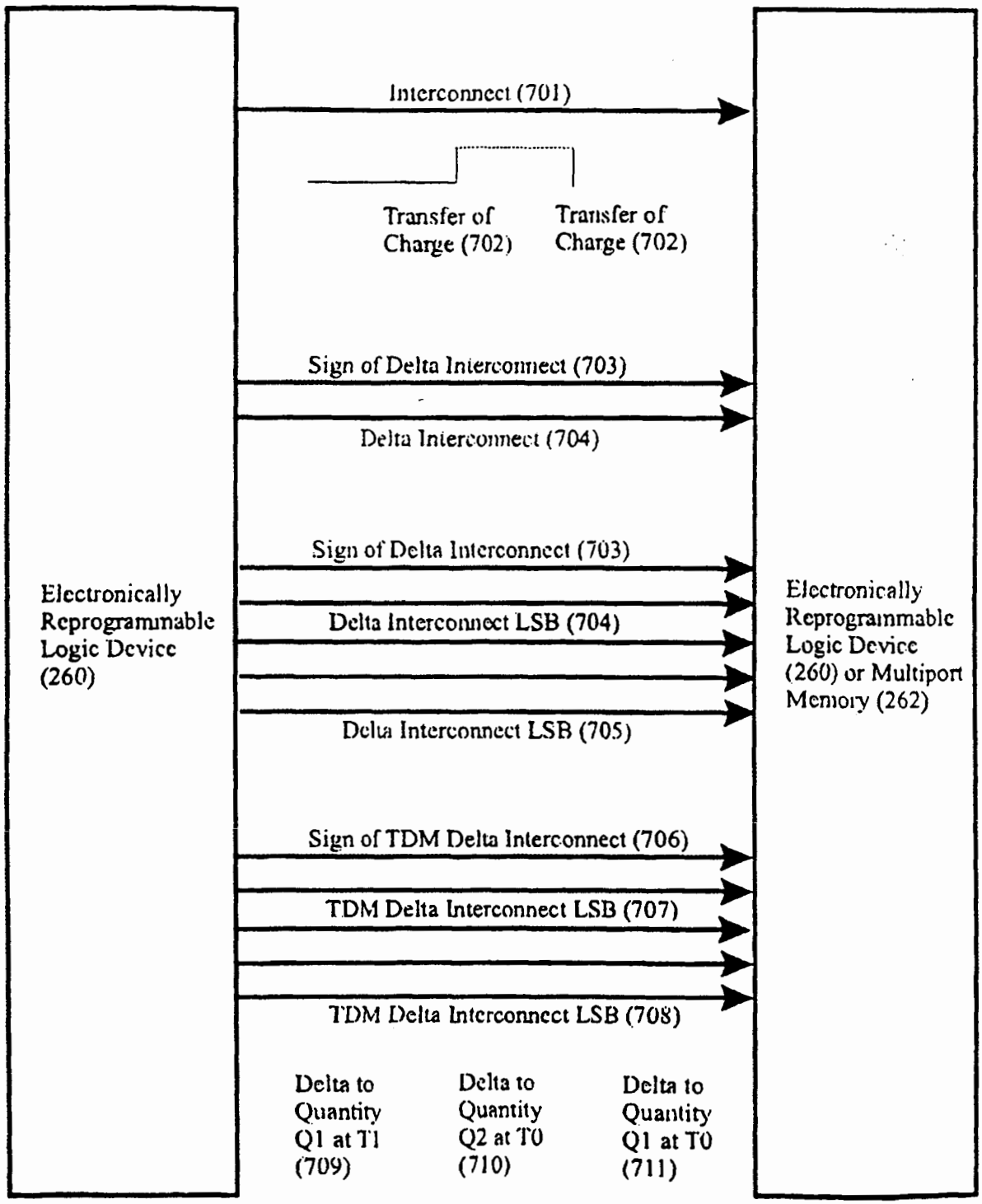
Drawing 14


Execute Analog Solver Partition (612)
Copy values of imported Analog Objects and Digital Objects from external memory to FPGA storage (600)
613
Duplicate Object Values when required to permit simultaneous computation of all expressions referencing Object Value (610)
615
616
Means of evaluating expressions on either side of an Inequality (602)
Means of evaluating expressions on either side of an Inequality (602)
617
618
Means of comparing the left and right hand side of an Inequality against the applicable tolerance (603)
Continue Iterating Context-Specific Analog Solver (629)
619
620
Context-Specific Analog Solver Converged (604)
Context Specific Analog Solver Beyond Tolerances (605)
621
622
623
Update integrals and differentials derived from Quantity values (606)
632
Copy exported Quantity and Derivative Quantity values to external memories (607)
Means of computing the global delta for each Quantity (608)
626
628
624
Execute Next Partition (609)
Means of applying the Global Delta for each Quantity to all representations of the Quantity (601)
627
630
Compute new DC Solution (629)
Re-evaluate the Operating Context and update the current Context-Specific Analog Solver (611)
631

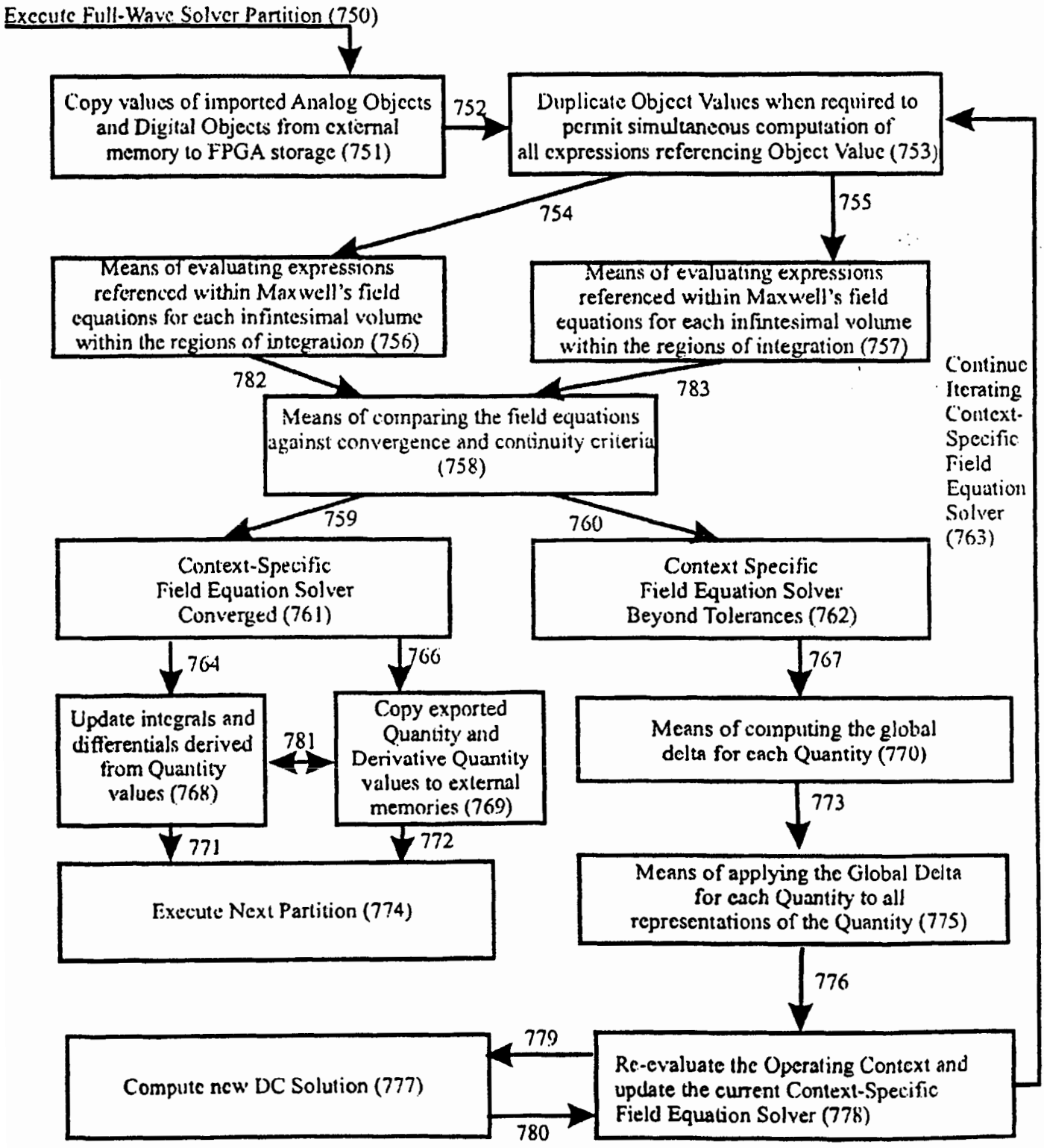
Drawing 15


Inter-Device Delta Signal (664)
Load / Store Value (663)
Multiplexor (669)
671
Read-only Literals (651)
Signal (652)
Shared Variable (653)
Quantity (654)
Terminal (655)
Temporary (656)
Delta (657)
Embedded Memory (650)
(665)
(664)
Temp Register (661)
(666)
Inter-Device Delta Signal (664)
Load / Store Value (663)
Multiplexor (669)
672
Read-only Literals (651)
Signal (652)
Shared Variable (653)
Quantity (654)
Terminal (655)
Temporary (656)
Delta (657)
Embedded Memory (660)
(665)
(664)
Temp Register (661)
(666)
Arithmetic Logic Unit (662)
Inter-Device Delta (670)
Condition Code (668)
(667)

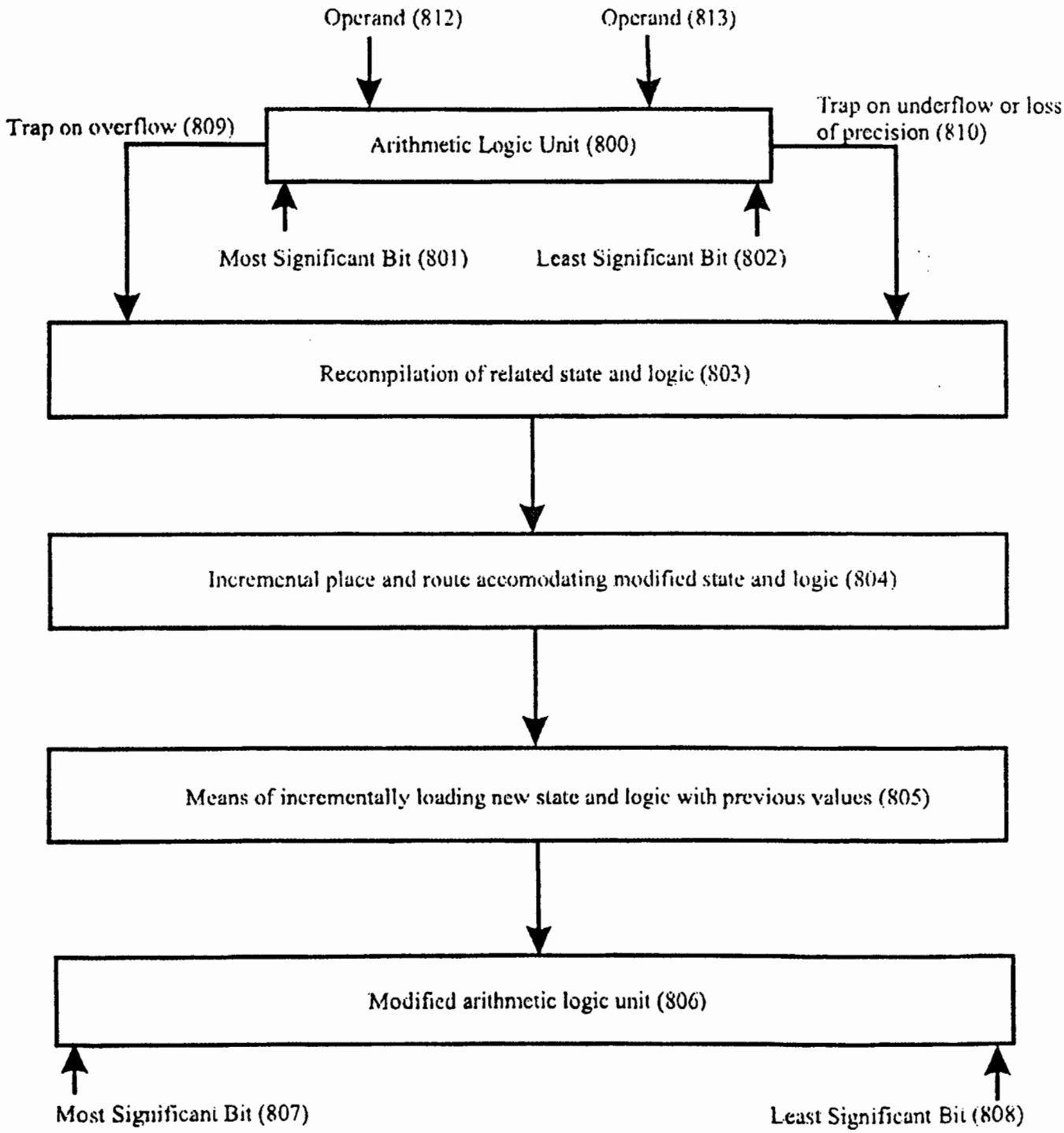
Drawing 16


Interconnect (701)
Transfer of Charge (702)
Transfer of Charge (702)
Sign of Delta Interconnect (703)
Delta Interconnect (704)
Sign of Delta Interconnect (703)
Delta Interconnect LSB (704)
Delta Interconnect LSB (705)
Sign of TDM Delta Interconnect (706)
TDM Delta Interconnect LSB (707)
TDM Delta Interconnect LSB (708)
Electronically Reprogrammable Logic Device (260)
Electronically Reprogrammable Logic Device (260) or Multiport Memory (262)
Delta to Quantity Q1 at T1 (709)
Delta to Quantity Q2 at T0 (710)
Delta to Quantity Q1 at T0 (711)

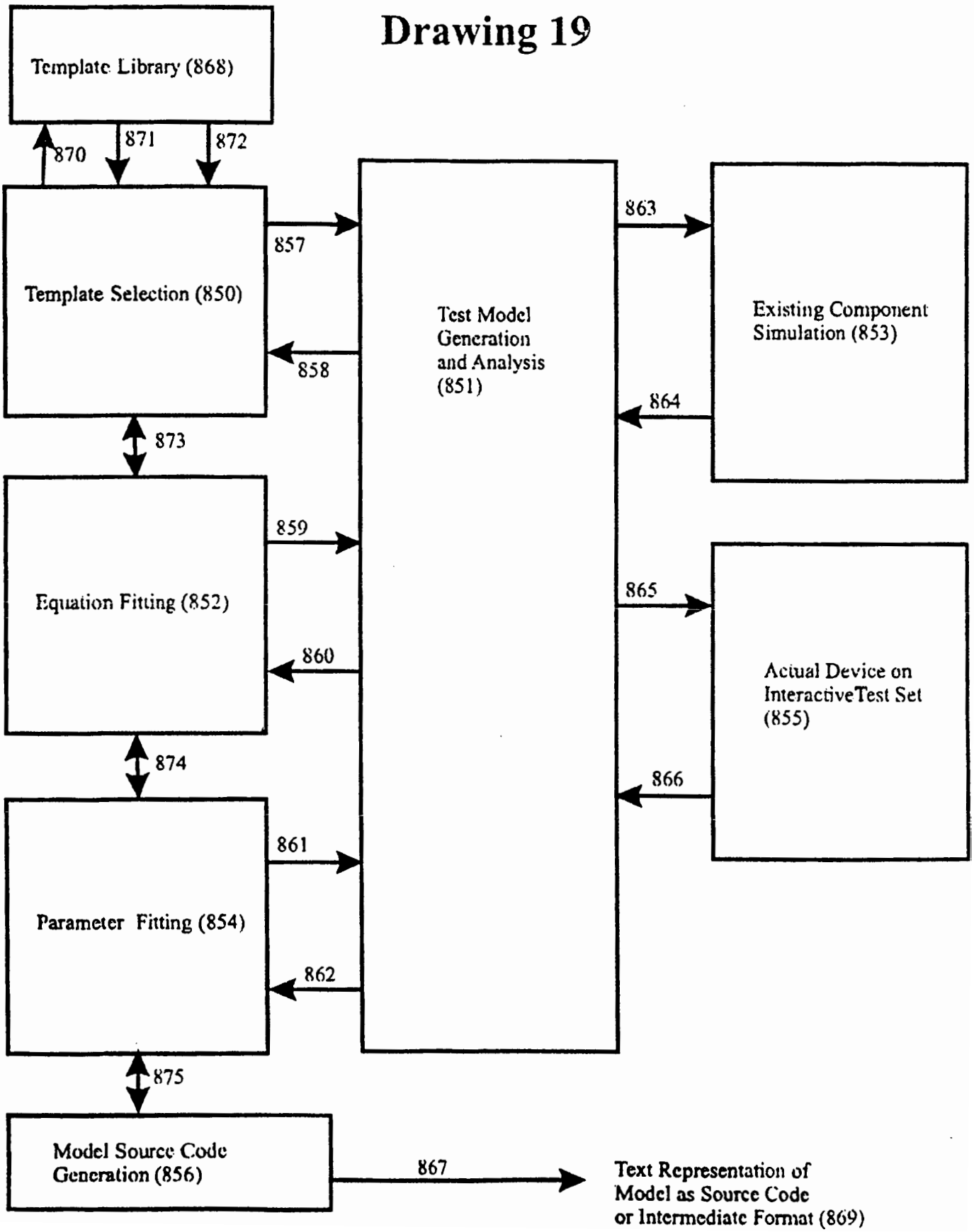
Drawing 17


Execute Full-Wave Solver Partition (750)
Copy values of imported Analog Objects and Digital Objects from external memory to FPGA storage (751)
752
Duplicate Object Values when required to permit simultaneous computation of all expressions referencing Object Value (753)
754
755
Means of evaluating expressions referenced within Maxwell's field equations for each infintesimal volume within the regions of integration (756)
Means of evaluating expressions referenced within Maxwell's field equations for each infintesimal volume within the regions of integration (757)
782
783
Means of comparing the field equations against convergence and continuity criteria (758)
Continue Iterating Context-Specific Field Equation Solver (763)
759
760
Context-Specific Field Equation Solver Converged (761)
Context Specific Field Equation Solver Beyond Tolerances (762)
764
766
767
Update integrals and differentials derived from Quantity values (768)
781
Copy exported Quantity and Derivative Quantity values to external memories (769)
Means of computing the global delta for each Quantity (770)
773
771
772
Execute Next Partition (774)
Means of applying the Global Delta for each Quantity to all representations of the Quantity (775)
776
779
Compute new DC Solution (777)
Re-evaluate the Operating Context and update the current Context-Specific Field Equation Solver (778)
780

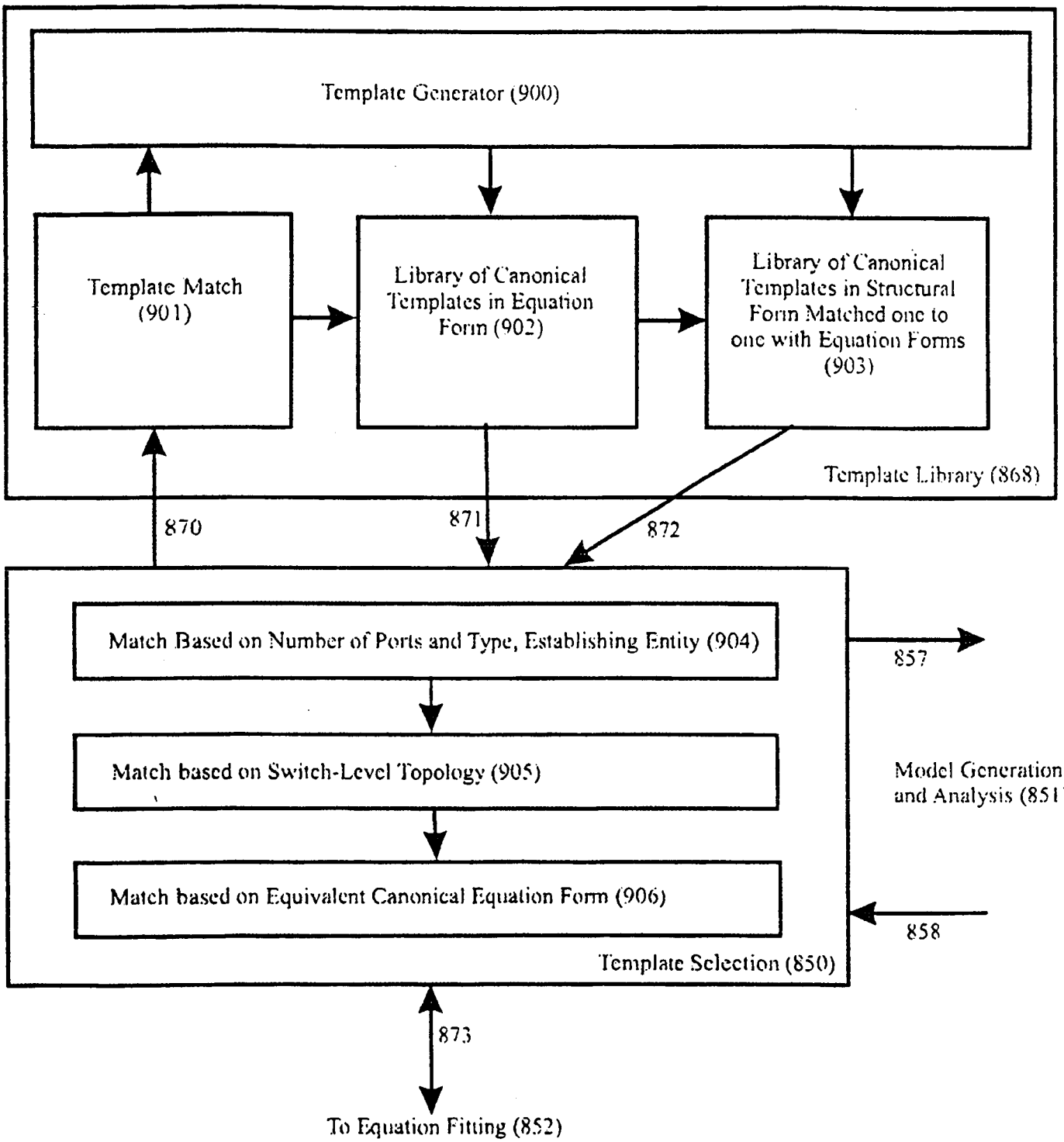
Drawing 18


Operand (812)
Operand (813)
Trap on overflow (809)
Arithmetic Logic Unit (800)
Trap on underflow or loss of precision (810)
Most Significant Bit (801)
Least Significant Bit (802)
Recompilation of related state and logic (803)
Incremental place and route accomodating modified state and logic (804)
Means of incrementally loading new state and logic with previous values (805)
Modified arithmetic logic unit (806)
Most Significant Bit (807)
Least Significant Bit (808)

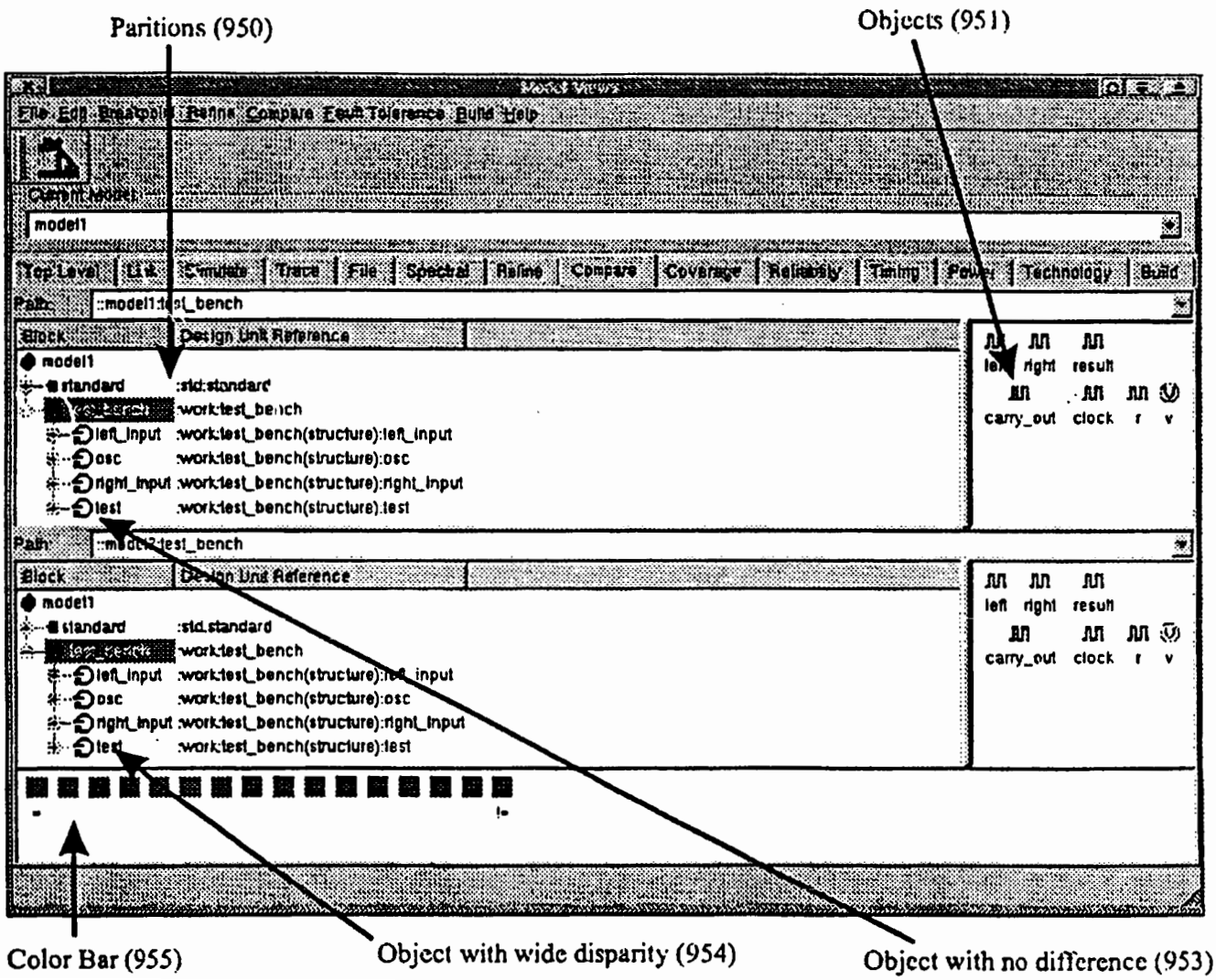
Drawing 19


Template Library (868)
870
871
872
Template Selection (850)
857
858
873
Equation Fitting (852)
859
860
874
Parameter Fitting (854)
861
862
875
Model Source Code Generation (856)
867
Text Representation of Model as Source Code or Intermediate Format (869)
Test Model Generation and Analysis (851)
863
864
Existing Component Simulation (853)
865
866
Actual Device on InteractiveTest Set (855)

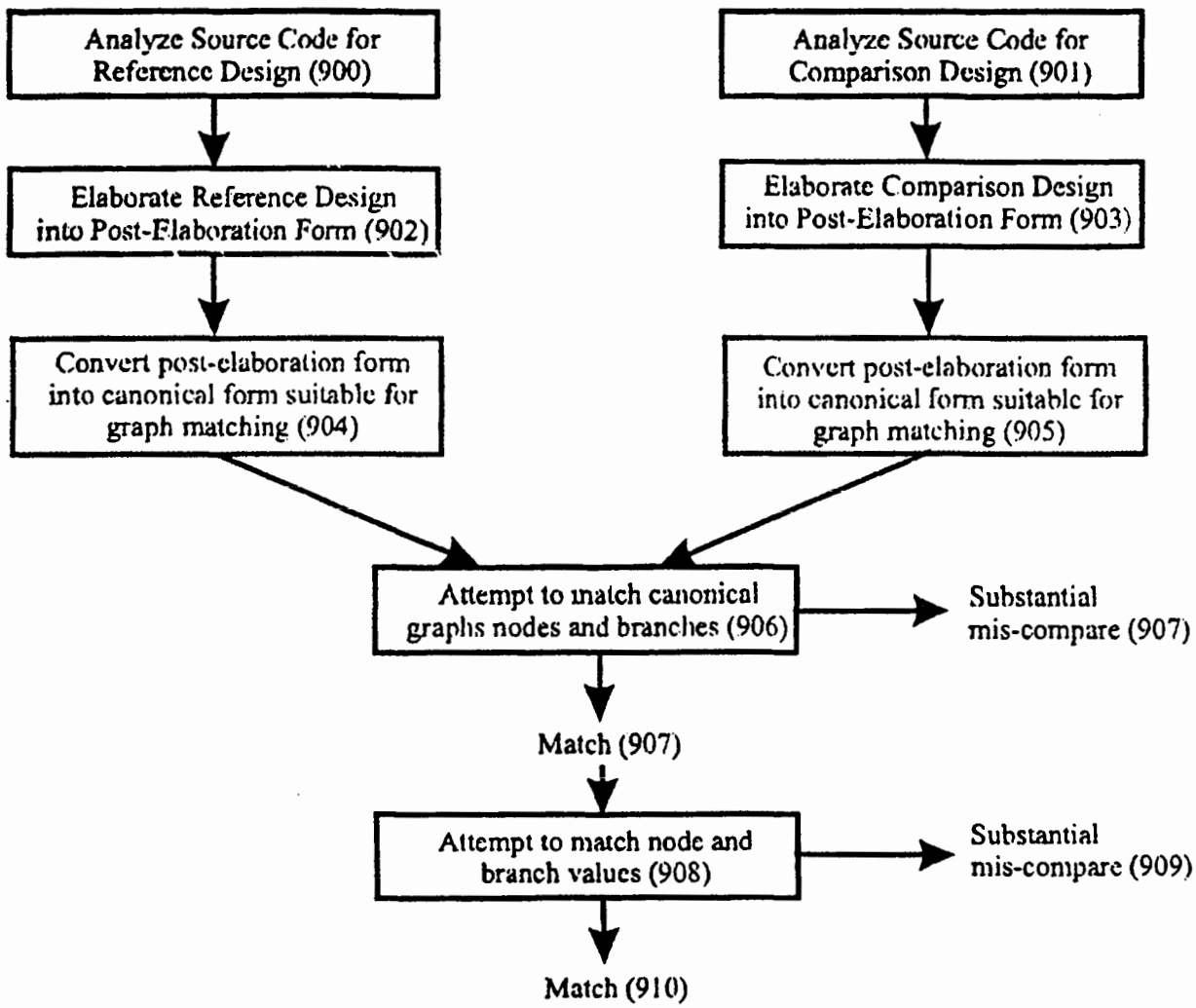
Drawing 20


Template Generator (900)
Template Match (901)
Library of Canonical Templates in Equation Form (902)
Library of Canonical Templates in Structural Form Matched one to one with Equation Forms (903)
Template Library (868)
870
871
872
Match Based on Number of Ports and Type, Establishing Entity (904)
Match based on Switch-Level Topology (905)
Match based on Equivalent Canonical Equation Form (906)
Template Selection (850)
857
858
Model Generation and Analysis (851)
873
To Equation Fitting (852)

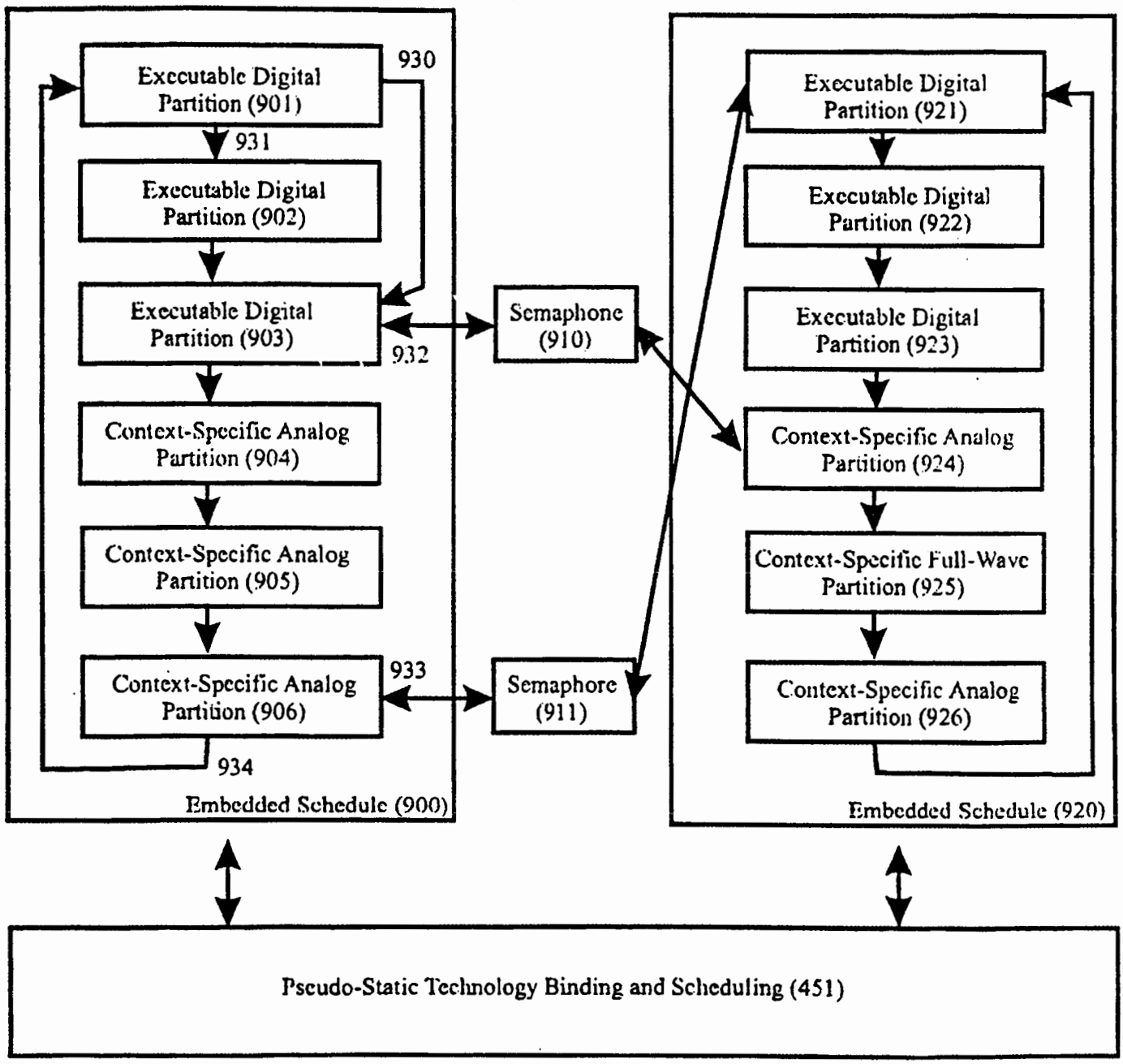
Drawing 21


Paritions (950)
Objects (951)
Color Bar (955)
Object with wide disparity (954)
Object with no difference (953)

Drawing 22


Analyze Source Code for Reference Design (900)
Analyze Source Code for Comparison Design (901)
Elaborate Reference Design into Post-Elaboration Form (902)
Elaborate Comparison Design into Post-Elaboration Form (903)
Convert post-elaboration form into canonical form suitable for graph matching (904)
Convert post-elaboration form into canonical form suitable for graph matching (905)
Attempt to match canonical graphs nodes and branches (906)
Substantial mis-compare (907)
Match (907)
Attempt to match node and branch values (908)
Substantial mis-compare (909)
Match (910)

Drawing 23


Executable Digital Partition (901)
930
931
Executable Digital Partition (902)
Executable Digital Partition (903)
932
Semaphone (910)
Context-Specific Analog Partition (904)
Context-Specific Analog Partition (905)
Context-Specific Analog Partition (906)
933
Semaphore (911)
934
Embedded Schedule (900)
Executable Digital Partition (921)
Executable Digital Partition (922)
Executable Digital Partition (923)
Context-Specific Analog Partition (924)
Context-Specific Full-Wave Partition (925)
Context-Specific Analog Partition (926)
Embedded Schedule (920)
Pseudo-Static Technology Binding and Scheduling (451)