# EFFICIENT TRANSISTOR STRUCTURE

## CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a continuation of U.S. Patent Application Nos. 11/524,113, filed September 20, 2006, 11/586,467, filed October 25, 2006, 11/586,470, filed October 25, 2006, 11/586,471, filed October 25, 2006, which applications claim the benefit of U.S. Provisional Application Nos. 60/825,517, filed September 13, 2006, 60/824,357, filed September 1, 2006, 60/823,332, filed on August 23, 2006, 60/821,008, filed August 1, 2006 and 60/798,568, filed on May 8, 2006. The disclosure of the above application is incorporated herein by reference in its entirety.

## FIELD OF THE INVENTION

[0002] The present invention relates to transistor structures, and more particularly to transistor structures with reduced chip area.

## BACKGROUND OF THE INVENTION

[0003] Integrated circuits or chips may include a large number of interconnected transistors. The transistors and other circuit elements are interconnected in various ways to provide desired circuit functions. It is usually most efficient to fabricate multiple integrated circuits on a single wafer. After processing, the integrated circuits that are fabricated on the wafer are separated and then packaged. The wafer can accommodate a fixed number of integrated circuits for a given integrated circuit size. Reducing the size of individual transistors in the integrated circuit may help to reduce the overall size of the integrated circuit. This, in turn, allows an increased number of integrated circuits or chips to be made on each wafer and reduces the cost of the integrated circuits.

[0004] Referring now to FIGs. 1 and 2, an exemplary transistor 10 includes a drain 12, a gate 14, a source 16 and a body 18 or substrate tap. For example, the transistor 10 in FIG. 1 is an NMOS transistor. In some circumstances, the body 18 is connected to the source 16 as shown in FIG. 2.

[0005] Referring now to FIG. 3, the body 18 includes a $p^+$ region and may include a contact tap 30. The source 16 includes an $n^+$ region and may include a contact tap 32. The drain 12 includes an $n^+$ region and may include a contact tap 34. Additional transistors may be fabricated on one or sides of the transistor 10 as indicated by "..." in FIG. 3.

[0006] Referring now to FIG. 4, the body 18 may be repeated between sources 16 of adjacent transistors. The body 18 takes up valuable chip area and increases the size of the transistor and the integrated circuit. Additional transistors can be arranged on one or more sides of the transistor 10 as shown by "..." in FIG. 4.

## SUMMARY OF THE INVENTION

[0007] An integrated circuit comprises a first source, a first drain, a second source, a first gate arranged between the first source and the first drain, and a second gate arranged between the first drain and the second source. The first and second gates define alternating first and second regions in the drain. The first and second gates are arranged farther apart in the first regions than in the second regions.

[0008] In other features, a well substrate contact is arranged in the first regions. Alternatively, R well substrate contacts are arranged in the first regions, where R is an integer greater than one. R is an integer that is greater than three and less than seven. The integrated circuit includes a plurality of transistors. The transistors include PMOS transistors. The R well substrate contacts are associated with respective ones of R transistors.

[0009] In other features, the integrated circuit comprises a second drain; and a third gate arranged between the second source and the second drain. The second and third gates define alternating third and fourth regions. The second and third gates are arranged farther apart in the third regions than in the fourth regions.

[0010] In yet other features, the first regions are arranged adjacent to the fourth regions and the second regions are arranged adjacent to the third regions. The first and third regions include R well substrate contacts.

[0011] A method for providing an integrated circuit comprises providing a first source; providing a first drain; providing a second source; locating a first gate between the first source and the first drain; locating a second gate between the first drain and the second source; defining alternating first and second regions in the drain using the first and second gates; and arranging the first and second gates farther apart in the first regions as compared to the second regions.

[0012] In other features, the method includes locating a well substrate contact in the first regions. The method includes locating R well substrate contacts in the first regions, where R is an integer greater than one. R is an integer that is greater than three and less than seven. The integrated circuit includes a plurality of transistors. The transistors include PMOS transistors. The method includes associating the R well substrate contacts with respective ones of R transistors.

[0013] In other features, the method includes providing a second drain; providing a third gate between the second source and the second drain; defining alternating third and fourth regions using the second and third gates; and arranging the second and third gates are arranged farther apart in the third regions than in the fourth regions.

[0014] In other features, the method includes arranging the first regions adjacent to the fourth regions and the second regions adjacent to the third regions. The first and third regions include R well substrate contacts, where R is an integer greater than one.

[0015] An integrated circuit comprises a first drain region having a generally rectangular shape. First, second, third and fourth source regions have a generally rectangular shape and are arranged adjacent to sides of the first drain region. A gate region is arranged between the first, second, third and fourth source regions and the first drain region. First, second, third and fourth substrate contact regions are arranged adjacent to corners of the first drain region.

[0016] In other features, the first, second, third and fourth source regions have a length that is substantially equal to a length of the drain region.

The first, second, third and fourth source regions have a width that is less than a width of the first drain region. The width of the first, second, third and fourth source regions is approximately one-half the width of the first drain region.

**[0017]** In other features, a second drain region has a generally rectangular shape and has one side that is arranged adjacent to the first source region. Fifth, sixth and seventh source regions have a generally rectangular shape. The fifth, sixth and seventh source regions are arranged adjacent to other sides of the second drain region.

**[0018]** In other features, a gate region is arranged between the first, fifth, sixth and seventh source regions and the second drain region. Fifth and sixth substrate contact regions are arranged adjacent to corners of the second drain region. The integrated circuit includes laterally-diffused MOSFET transistors.

**[0019]** A method for providing an integrated circuit comprises providing a first drain region having a generally rectangular shape; arranging sides of first, second, third and fourth source regions, which have a generally rectangular shape, adjacent to sides of the first drain region; arranging a gate region between the first, second, third and fourth source regions and the first drain region; and arranging first, second, third and fourth substrate contact regions adjacent to corners of the first drain region.

**[0020]** In other features, the first, second, third and fourth source regions have a length that is substantially equal to a length of the drain region. The first, second, third and fourth source regions have a width that is less than a width of the first drain region. The width of the first, second, third and fourth source regions is approximately one-half the width of the first drain region.

**[0021]** In other features, the method includes arranging one side of a second drain region, which has a generally rectangular shape, adjacent to the first source region; and arranging fifth, sixth and seventh source regions, which have a generally rectangular shape, adjacent to other sides of the second drain region. The method includes arranging a gate region between the first, fifth, sixth and seventh source regions and the second drain region. The method includes arranging fifth and sixth substrate contact regions adjacent to corners of

the second drain region. The integrated circuit includes laterally-diffused MOSFET transistors.

[0022] An integrated circuit comprises a first drain region having a symmetric shape across at least one of horizontal and vertical centerlines. A first gate region has a first shape that surrounds the first drain region. A second drain region has the symmetric shape. A second gate region has the first shape that surrounds the second drain region. A connecting gate region connects the first and second gate regions. A first source region is arranged adjacent to and on one side of the first gate region, the second gate region and the connecting gate region. A second source region is arranged adjacent to and on one side of side of the first gate region, the second gate region and the connecting gate region.

[0023] In other features, the symmetric shape tapers as a distance from a center of the symmetric shape increases. First and second substrate contacts are arranged in the first and second source regions. The integrated circuit includes laterally-diffused MOSFET transistors.

[0024] In other features, the symmetric shape is a circular shape. The symmetric shape is an elliptical shape. The symmetric shape is a polygonal shape. The symmetric shape is a hexagonal shape.

[0025] A method for providing an integrated circuit comprises providing a first drain region having a symmetric shape across at least one of horizontal and vertical centerlines; providing a first gate region having a first shape that surrounds the first drain region; providing a second drain region having the symmetric shape; providing a second gate region having the first shape that surrounds the second drain region; connecting a connecting gate region to the first and second gate regions; arranging a first source region adjacent to and on one side of the first gate region, the second gate region and the connecting gate region; and arranging a second source region adjacent to and on one side of side of the first gate region, the second gate region and the connecting gate region.

[0026] In other features, the symmetric shape tapers as a distance from a center of the symmetric shape increases. In other features, the method

includes arranging first and second substrate contacts in the first and second source regions. The integrated circuit includes laterally-diffused MOSFET transistors.

**[0027]** In other features, the symmetric shape is a circular shape. The symmetric shape is an elliptical shape. The symmetric shape is a polygonal shape. The symmetric shape is a hexagonal shape.

**[0028]** An integrated circuit comprises first and second drain regions having a generally rectangular shape. First, second and third source regions that have a generally rectangular shape, wherein the first source region is arranged between first sides of the first and second drain regions and the second and third source regions are arranged adjacent to second sides of the first and second drain regions. A fourth source region is arranged adjacent to third sides of the first and second drain regions. A fifth source region is arranged adjacent to fourth sides of the first and second drain regions. A gate region is arranged between the first, second, third, fourth and fifth source regions and the first and second drain regions. First and second drain contacts are arranged in the first and second drain regions.

**[0029]** A method for providing an integrated circuit comprises providing first and second drain regions having a generally rectangular shape; arranging a first source region between first sides of the first and second drain regions; arranging second and third source regions adjacent to second sides of the first and second drain regions; arranging a fourth source region adjacent to third sides of the first and second drain regions; arranging a fifth source region adjacent to fourth sides of the first and second drain regions; arranging a gate region between the first, second, third, fourth and fifth source regions and the first and second drain region; and arranging first and second drain contacts in the first and second drain regions.

**[0030]** In other features of the integrated circuit and method, the first, second and third source regions have a length that is substantially equal to a length of the first drain region and wherein the fourth and fifth source regions have a length that is greater than or equal to a length of the first and second drain regions. The first, second and third source regions have a width that is

less than a width of the first drain region. The width of the first, second and third source regions is approximately one-half the width of the first drain region. The fourth and fifth source regions are driven from sides thereof. The first and second drain contacts have a size that is greater than a minimum drain contact size. The drain contacts have one of a regular shape and an irregular shape. The drain contacts are one of square, rectangular, and cross-shaped. The first, second and third source regions include source contacts. The first and second drain regions and the firs, second and third source regions are arranged in a first row and further comprising N additional rows, wherein drain regions of at least one of the N additional rows share one of the fourth and fifth source regions.

**[0031]** An integrated circuit comprises first and second drain regions having a generally rectangular shape. First, second and third source regions that have a generally rectangular shape, wherein the first source region is arranged between first sides of the first and second drain regions and the second and third source regions are arranged adjacent to second sides of the first and second drain regions. A fourth source region is arranged adjacent to third sides of the first and second drain regions. A fifth source region is arranged adjacent to fourth sides of the first and second drain regions. A gate region is arranged between the first, second, third, fourth and fifth source regions and the first and second drain regions. First and second drain contacts are arranged in the first and second drain regions.

**[0032]** A method for providing an integrated circuit comprises providing first and second drain regions having a generally rectangular shape; arranging a first source region between first sides of the first and second drain regions; arranging second and third source regions adjacent to second sides of the first and second drain regions; arranging a fourth source region adjacent to third sides of the first and second drain regions; arranging a fifth source region adjacent to fourth sides of the first and second drain regions; arranging a gate region between the first, second, third, fourth and fifth source regions and the first and second drain region; and arranging first and second drain contacts in the first and second drain regions.

[0033] In other features of the integrated circuit and method, the first, second and third source regions have a length that is substantially equal to a length of the first drain region and wherein the fourth and fifth source regions have a length that is greater than or equal to a length of the first and second drain regions. The first, second and third source regions have a width that is less than a width of the first drain region. The width of the first, second and third source regions is approximately one-half the width of the first drain region. The fourth and fifth source regions are driven from sides thereof. The first and second drain contacts have a size that is greater than a minimum drain contact size. The drain contacts have one of a regular shape and an irregular shape. The drain contacts are one of square, rectangular, and cross-shaped. The first, second and third source regions include source contacts. The first and second drain regions and the firs, second and third source regions are arranged in a first row and further comprising N additional rows, wherein drain regions of at least one of the N additional rows share one of the fourth and fifth source regions.

[0034] Further regions of applicability of the present invention will become apparent from the detailed description provided hereinafter. It should be understood that the detailed description and specific examples, while indicating the preferred embodiment of the invention, are intended for purposes of illustration only and are not intended to limit the scope of the invention.

## BRIEF DESCRIPTION OF THE DRAWINGS

[0035] The present invention will become more fully understood from the detailed description and the accompanying drawings, wherein:

[0036] FIG. 1 is an electrical symbol for a transistor with a drain, source, gate and body according to the prior art;

[0037] FIG. 2 is an electrical symbol for a transistor with a drain, source, gate and body, which is connected to the source according to the prior art;

[0038] FIG. 3 is an exemplary layout of the transistor of FIG. 2 according to the prior art;

[0039] FIG. 4 is an exemplary layout of multiple transistors that are arranged in a row according to the prior art;

[0040] FIG. 5A is a first exemplary layout of transistors including a body that is arranged in the source;

[0041] FIG. 5B is a second exemplary layout of transistors including a body having edges that align with the gates in plan view;

[0042] FIG. 6 is a second exemplary layout of transistors including a body that is arranged in the source;

[0043] FIG. 7 is a third exemplary layout of transistors including a body that is arranged in the source;

[0044] FIG. 8 is a fourth exemplary layout of transistors including a body that is arranged in the source;

[0045] FIG. 9 is a fifth exemplary layout of transistors including a body that is arranged in the source;

[0046] FIG. 10 is a cross-sectional view of a PMOS transistor according to the prior art;

[0047] FIG. 11 is a plan view of a sixth exemplary layout including well substrate contacts;

[0048] FIG. 12A is a plan view of a seventh exemplary layout for reducing $R_{DSon}$;

[0049] FIG. 12B is a plan view of the seventh exemplary layout of FIG. 12A;

[0050] FIG. 12C is a plan view of an eighth exemplary layout for reducing $R_{DSon}$;

[0051] FIG. 12D is a plan view of a ninth exemplary layout for reducing $R_{DSon}$ that is similar to FIG. 12C;

[0052] FIG. 12E is a plan view of a tenth exemplary layout for reducing $R_{DSon}$ that is similar to FIG. 12C;

[0053] FIGs. 12F-12I illustrate other exemplary drain contacts;

[0054] FIG. 13 is a plan view of a eleventh exemplary layout for reducing $R_{DSon}$; and;

[0055] FIG. 14 is a plan view of a twelfth exemplary layout for reducing $R_{DSon}$;

[0056] FIG. 15 is a plan view of a thirteenth exemplary layout for reducing $R_{DSon}$;

[0057] FIG. 16A is a functional block diagram of a hard disk drive;

[0058] FIG. 16B is a functional block diagram of a DVD drive;

[0059] FIG. 16C is a functional block diagram of a high definition television;

[0060] FIG. 16D is a functional block diagram of a vehicle control system;

[0061] FIG. 16E is a functional block diagram of a cellular phone;

[0062] FIG. 16F is a functional block diagram of a set top box; and

[0063] FIG. 16G is a functional block diagram of a media player.

## DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0064] The following description of the preferred embodiment(s) is merely exemplary in nature and is in no way intended to limit the invention, its application, or uses. For purposes of clarity, the same reference numbers will be used in the drawings to identify the same elements. Additional transistors can be arranged on one or more sides of the illustrated transistors that are shown in the FIGs. as indicated by "..." in the FIGs.

[0065] Referring now to FIGs. 5A and 5B, a transistor 50 according to the present invention is shown to include one or more sources 54 and one or more drains 56. The sources 54 and the drains 56 include $n^+$ regions. While an NMOS transistor is shown, skilled artisans will appreciate that the present invention also applies to other types of transistors such as PMOS transistors. Gates 58 are located between adjacent pairs of sources 54 and drains 56. In one implementation, the gates 58 that are located on opposite sides of the sources 54 are connected together as shown at 64. In other configurations, however, the gates 58 need not be connected together.

[0066] A body 66 including a $p^+$ region is arranged inside of and is surrounded by the source 54. The body 66 preferably has a shape that tapers

as a distance between a midportion of the body 66 and adjacent gates decreases. The body 66 may touch or not touch the gates 58 in the plan views of FIGs. 5A and 5B. In other words, one or both edges of the body 66 may be spaced from the gates 58 in plan view (as shown in FIG. 5A) and/or substantially aligns with the gates in plan view (as shown in FIG. 5B). By utilizing some of the area of the source 54 for the body 66, the overall size of the transistor 50 is reduced as compared to conventional transistors. In the exemplary implementation that is shown in FIG. 5, the body 66 has a diamond shape.

**[0067]** Referring now to FIGs. 6 and 7, other exemplary shapes for the body 66 are shown. In FIG. 6, the body 66 has a hexagon shape. In FIG. 7, the body is generally football shaped. Skilled artisans will appreciate that there are a wide variety of other suitable shapes. For example, a circular body is shown in FIG. 8, which is described. Other suitable shapes include an ellipse, an octagon, etc.

**[0068]** Referring now to FIGs. 8 and 9, the gates 58 can be arranged such that they are closer together when there are no contact taps and further apart when there are contact taps. In FIG. 8, a source contact tap 70, which is not located in the body 66, is located in a region where the adjacent gates 58 are located farther apart. In FIG. 9, a body contact tap 80, which is located in the body 66, is located in the source 54 where the adjacent gates 58 are located farther apart.

**[0069]** Referring now to FIG. 10, a PMOS transistor 120 is shown. The transistor 120 includes a gate contact 122, a source contact 126, a drain contact 128 and a negative (N)-well contact 130. The source contact 126 provides a connection to a P++ region 134 formed an N-type substrate layer 138. The N-type layer 138, in turn, is formed in a P-type substrate 140. The P++ region 134 forms the source. The drain contact 128 provides an electrical connection to a P++ region 136 formed in the N-type layer 138. The P++ region 136 forms the drain. The N-well contact 130 provides a connection to an N++ region 141 or N-well.

**[0070]** Referring now to FIG. 11, a plan view of a sixth exemplary layout is shown. For some transistor designs such as PMOS and/or NMOS

transistors, electrostatic discharge (ESD) is less important than other design criteria. Therefore, N-well contact areas can be minimized. For PMOS transistors, the N-well contact area may be approximately 2.5 to 3 times the area in NMOS transistors. The source-drain resistance may be less important. Therefore, the layout in FIG. 11 minimizes the N-well contact areas and the source-drain area. Skilled artisans will appreciate that while the foregoing description relates to PMOS transistors, similar principles apply to NMOS transistors.

**[0071]** In a layout shown in FIG. 11, gate regions 200-1, 200-2, ..., and 200-G (collectively gate regions or gates 200) are defined between source regions 224-1, 224-2, ..., and 224-S (collectively source regions 224) and drain regions 220-1, 220-2, ..., and 220-D (collectively drain regions 220). Adjacent gates 200-1 and 200-2 define regions 210 having a wider width than adjacent regions 212 having narrower widths. Drain regions 220 and source regions 224 are alternately defined between the adjacent gates 200.

**[0072]** Groups of transistors 230-11, 230-12, ..., and 230-XY (collectively groups of transistors 230) are arranged adjacent to each other. Adjacent groups of transistors 230 share R N-well contacts 260, where R is an integer greater than one. The R N-well contacts 260 can be located between the adjacent groups of transistors 230 in regions 210 where the gates 200 are spaced further apart.

**[0073]** The source-drain area is minimized by this layout. For example, each group may include 4-6 transistors. The R N-well contacts 260 are provided for adjacent groups in both vertical and horizontal directions. Therefore, abutting edges of the adjacent groups without the R N-well contacts 260 can be located in regions 212 where the gates are spaced closer together. In other words, the gates 200 can be arranged closer together to minimize areas of the regions 212 without the R N-well contacts 260.

**[0074]** Referring now to FIG. 12A, an exemplary high-density layout for laterally diffused MOSFET (LDMOS) transistors 300 is shown. The layout tends to reduce turn-on drain-source resistance $R_{DSon}$. The transistors 300 include source (S) regions 304, drain (D) regions 306 and gates 310. Some, none or all

of the source regions 304 may include one or more source contacts 311. For illustration purposes, not all of the source regions 304 are shown with source contacts 311.

**[0075]** The gates 310 define a checkerboard pattern. Source regions 304 are arranged along sides of the drain regions 306. More particularly, the drain regions 306 may have a generally rectangular shape. The source regions 304 may be arranged along each side of the generally rectangular drain regions 306. Substrate contacts 330 may be provided adjacent to corners of the drain regions 306 at intersections between adjacent source regions 304. Drain contacts 334 may also be provided at a central location within the drain regions 306.

**[0076]** Each drain region 306 may be arranged adjacent to source regions 304 that are common with other adjacent drain regions 306. For example in dotted area 331 in FIG. 12A, drain region 306-1 shares the source region 304-1 with the drain region 306-2. Drain region 306-1 shares the source region 304-2 with the drain region 306-3. Drain region 306-1 shares the source region 304-3 with the drain region 306-4. Drain region 306-1 shares the source region 304-4 with the drain region 306-5. This pattern may be repeated for adjacent drain regions 306.

**[0077]** Each of the drain regions 306 may have an area that is greater than or equal to two times the area of each of the source regions 304. In FIG. 12A, the drain regions 306 have a width "b" and a height "a". The source regions 304 have a width (or height) "d" and a height (or width) "c". The drain regions 306 may have substantially the same length as the source regions 304. The drain regions 306 may have greater than or equal to two times the width of the source regions 304.

**[0078]** Referring now to FIG. 12B, a more detailed view of part of the layout of FIG. 12A is shown. Drain contacts 334-1 and 334-3 may be associated with drain regions 306-1 and 306-3, respectively. Substrate contacts 330 are located adjacent to corners of the drain regions 306-1. Source contacts 311-1, 311-2, ... and 311-B may be arranged in source regions 304-2 and 304-4, where B is an integer. Drain contacts 334-1 and 334-3 may be arranged in each of the

drain regions 306-1 and 306-3, respectively. Drain contact 334-1 may define an area that is greater than the area of the source contact 311-1 in the source region 304-2.

**[0079]** Substantially all of the current flowing between the drain region 306-3 and the source contacts 311-1, 311-2, ... and 311-B of the adjacent source region 304-2 flows between a facing portion 335 of the drain contact 334-3 and facing halves 337-1, 337-2, ... and 337-S of source contacts 311-1, 311-2, ... and 311-B in the source region 304-2. Current flows in a similar manner between other facing portions of the drain contact 334-3 and source contacts (not shown) in other adjacent source regions 304-5, 304-6 and 304-7.

**[0080]** Referring now to FIG. 12C, another exemplary high-density layout for laterally diffused MOSFET (LDMOS) transistors 340 is shown. The layout tends to provide low turn-on drain-source resistance $R_{DSon}$. The transistors 340 include source regions 304-11, 304-12, ... 304-4Q, drain regions 306-11, 306-12, ... 306-4T and gates 310, where Q and T are integers. While four rows are shown in FIG. 12B, additional and/or fewer rows and/or columns may be employed. Some, none or all of the source regions 304 may include source contacts 311. For illustration purposes, not all of the source regions 304 are shown with source contacts. For example, source region 304-12 includes source contacts 311-1, 311-2, ... and 311-B, where B is an integer.

**[0081]** Other elongated source regions 344-1, 344-2, 344-3, ... and 344-R are arranged between rows (or columns) of drain regions 306 and may be driven by drivers 346-1, 346-2, ..., and 346-R arranged on one or both sides (or tops) of the layout in FIG. 12B. The elongated source regions 344-1, 344-2, 344-3, ... and 344-R may extend adjacent to sides of at least two drain regions 306 such as at least drain regions 306-11 and 306-12.

**[0082]** Each of the drain regions 306 (such as drain region 306-11) may have an area that is greater than or equal to two times the area of each of the source regions 304 (such as source region 304-12). The drain regions 306 (such as drain region 306-11) may have substantially the same length as the source regions 304 (such as source region 304-12). The drain regions 306

(such as drain region 306-11) may have greater than or equal to two times the width of the source regions 304 (such as source region 304-12).

**[0083]** Substrate contacts 347-11, 347-12, 347-21, 347-22, 347-23, ... 347-51, 347-52 (collectively substrate contacts 347) may be arranged in some, none or all of the elongated source regions 344. The placement and number of substrate contracts 347 may be uniform or varied for each of the elongated source regions 344. For example only, the substrate contacts 347 shown in FIG. 12C may be offset from the substrate contacts 347 in adjacent elongated source regions 344. Each of the elongated source regions 344 may include the same number or a different number of substrate contacts 347 than adjacent elongated source regions 344. The substrate contacts 347 may be aligned or offset as shown. Some elongated source regions 344 may include no substrate contacts 347. Still other variations are contemplated.

**[0084]** Referring now to FIG. 12D, first areas 345-A1, 345-A2, 345-A3 and 345-A4 may provide useful transistor areas. For example, first areas 345-A1, 345-A2, 345-A3 and 345-A4 may be located between drain region 306-12 and source regions 304-12, 344-1, 304-13, and 344-2, respectively. Second areas 345-B1, 345-B2, 345-B3 and 345-B4 may provide less useful transistor areas. For example, second areas 345-B1, 345-B2, 345-B3 and 345-B4 may be located between source regions 304-12, 344-1, 304-13, and 344-2.

**[0085]** In some implementations, the substrate contacts 347-11, 347-12, 347-21, 347-22, 347-23, ... may be arranged in some, none or all of the second areas 345-B1, 345-B2, 345-B3 and 345-B4 of the source regions 344-1, 344-2, ... and 344-R, for example as shown in FIG. 12D. The substrate contacts 347-11, 347-12, 347-21, 347-22, 347-23, ... are shown arranged in the elongated substrate regions 344-1 and 344-2 and tend to lower $R_{DS_ON}$. The substrate contacts 347-11, 347-12, 347-21, 347-22, 347-23, ... may have a height that is less than or equal to a width "c" of the source regions 304 (as shown in FIG. 12A) and a width that is less than or equal to a width "d" of the source regions 304 (as shown in FIG. 12A).

**[0086]** Referring now to FIG. 12E, substrate contacts 330-1 and 330-2 are provided between pairs of elongated source regions 344-1A and 344-1B and

344-2A and 344-2B, respectively. The elongated source regions 344-1A and 344-2A are driven from one side by drivers 346-1A and 346-2A. The elongated source regions 344-1B and 344-2B are driven from another side by drivers 346-1B and 346-2B.

[0087] . Drain contacts 334 in FIGs. 12A-12E may have a minimum size or a size that is greater than the minimum size. Drain contacts 334 may have a simple or regular shape and/or an irregular or complex shape. For example, the drain contacts 334 may have a square or rectangular shape (as shown at 344 in FIG. 12A), a cross shape (as shown at 344-W in FIG. 12F), clover-leaf shapes (as shown at 334-X and 334-Y in FIGs. 12G and 12H, respectively), a modified cross-shaped region (as shown at 334-Z in FIG. 12I) and/or other suitable shapes such as but not limited to diamond, circular, symmetric, non-symmetric, etc.. The substrate contacts 347 may similarly have a simple or regular shape and/or an irregular or complex shape similar to the drain contacts 334.

[0088] In some implementations, the number of source contacts B in a given source region may be an integer that is greater than one and less than six. In some implementations, B may be equal to 3 or 4. The area of the drain contact 334-3 may be greater than or equal to 2*B* (the area one of source contacts 311-1, 311-2, ... or 311-B). For example, when B is equal to 3, the drain contact region 334-3 may have an area that is approximately greater than or equal to 6 times an area of one source contact 311-1, 311-2, ... or 311-B. When B is equal to 4, the drain contact region 334-3 may an area that is approximately greater than or equal to 8 times an area of one source contact 311-1, 311-2, ... or 311-B.

[0089] As the size of the drain contacts 334 increases relative to the corresponding drain region 306, over-etching may occur. In other words, the etching process may adversely impact adjacent regions and/or underlying layers. To alleviate the problems of over-etching, the complex shapes in FIGs. 12F-12I and/or other complex shapes can be employed for the drain contacts 334. Alternately, the drain contacts 334 can employ deep implant ions in and/or below the drain contacts 334.

[0090] As an alternative to placing the substrate contact 330 in the elongated source regions 344, a relief area may be provided in one or both sides of the source region 344 in areas 345-B1, 345-B2, 345-B3 and 345-B. A substrate contact region 330 can be positioned in the relief area. The shape of the elongate source region 344 can be adjusted on an opposite side of the relief area to offset the effect of the relief area and to prevent reduction in current density in areas of the elongate source region 344 near the relief areas.

[0091] Referring now to FIGs. 13-15, drain, source and gate regions can also have other shapes that can be used to minimize $R_{DSON}$. For example, drain regions 348 can have a circular shape as shown in FIG. 13, an elliptical shape as shown in FIG. 14 and/or other suitable shapes. Gate regions 349 include circular-shaped gate regions 350 that are connected by linear gate connecting regions 352. Similar elements are identified in FIG. 14 using a prime symbol (" ' "). The drain regions 348 are located in the circular-shaped gate regions 350. Source regions 360 are located in between the gate regions 349 in areas other than the inside of the circular shaped gate regions 350. Substrate contacts 364 are located in the source regions 360. The drain regions 348 may also include a contact region 366. The linear gate regions 352 may have a vertical spacing "g" that is minimized to increase density. Likewise, lateral spacing identified at "f" between adjacent circular-shaped gate regions 350 may be minimized to increase density.

[0092] Drain areas 368 can also have polygon shapes. For example, the drain areas can have a hexagon shape as shown in FIG. 15, although other polygon shapes can be used. Gate regions 369 include hexagon-shaped gate regions 370 that are connected by linear gate connecting regions 372. The drain regions 368 are located in the hexagon-shaped gate regions 370. Source regions 380 are located in between the gate regions 369 in areas other than the inside of the hexagon-shaped gate regions 370. Substrate contacts 384 are located in the source regions 380. The drain regions may also include a contact region 386. The linear gate connecting regions 372 preferably have a vertical spacing "j" that is minimized to increase density. Likewise lateral spacing

identified at "i" between adjacent hexagon-shaped gate regions 370 is minimized to increase density.

**[0093]** As can be appreciated, the shapes for the drain and gate areas in FIGs. 13-15 can be any shape that is symmetric about at least one of the horizontal and vertical centerlines of the drain areas. The transistors in FIGs. 13-15 may be LDMOS transistors. The shape of the drain regions may include any symmetric shape. The shape may taper as a distance from a center point of the drain area increases and/or as a center point of the drain area increases in a direction towards one or more other transistors.

**[0094]** Referring now to FIGs. 16A-16G, various exemplary implementations incorporating the teachings of the present disclosure are shown.

**[0095]** Referring now to FIG. 16A, the teachings of the disclosure can be implemented in a transistors of a hard disk drive (HDD) 400. The HDD 400 includes a hard disk assembly (HDA) 401 and a HDD PCB 402. The HDA 401 may include a magnetic medium 403, such as one or more platters that store data, and a read/write device 404. The read/write device 404 may be arranged on an actuator arm 405 and may read and write data on the magnetic medium 403. Additionally, the HDA 401 includes a spindle motor 406 that rotates the magnetic medium 403 and a voice-coil motor (VCM) 407 that actuates the actuator arm 405. A preamplifier device 408 amplifies signals generated by the read/write device 404 during read operations and provides signals to the read/write device 404 during write operations.

**[0096]** The HDD PCB 402 includes a read/write channel module (hereinafter, "read channel") 409, a hard disk controller (HDC) module 410, a buffer 411, nonvolatile memory 412, a processor 413, and a spindle/VCM driver module 414. The read channel 409 processes data received from and transmitted to the preamplifier device 408. The HDC module 410 controls components of the HDA 401 and communicates with an external device (not shown) via an I/O interface 415. The external device may include a computer, a multimedia device, a mobile computing device, etc. The I/O interface 415 may include wireline and/or wireless communication links.

[0097] The HDC module 410 may receive data from the HDA 401, the read channel 409, the buffer 411, nonvolatile memory 412, the processor 413, the spindle/VCM driver module 414, and/or the I/O interface 415. The processor 413 may process the data, including encoding, decoding, filtering, and/or formatting. The processed data may be output to the HDA 401, the read channel 409, the buffer 411, nonvolatile memory 412, the processor 413, the spindle/VCM driver module 414, and/or the I/O interface 415.

[0098] The HDC module 410 may use the buffer 411 and/or nonvolatile memory 412 to store data related to the control and operation of the HDD 400. The buffer 411 may include DRAM, SDRAM, etc. The nonvolatile memory 412 may include flash memory (including NAND and NOR flash memory), phase change memory, magnetic RAM, or multi-state memory, in which each memory cell has more than two states. The spindle/VCM driver module 414 controls the spindle motor 406 and the VCM 407. The HDD PCB 402 includes a power supply 416 that provides power to the components of the HDD 400.

[0099] Referring now to FIG. 16B, the teachings of the disclosure can be implemented in a transistors of a DVD drive 418 or of a CD drive (not shown). The DVD drive 418 includes a DVD PCB 419 and a DVD assembly (DVDA) 420. The DVD PCB 419 includes a DVD control module 421, a buffer 422, nonvolatile memory 423, a processor 424, a spindle/FM (feed motor) driver module 425, an analog front-end module 426, a write strategy module 427, and a DSP module 428.

[0100] The DVD control module 421 controls components of the DVDA 420 and communicates with an external device (not shown) via an I/O interface 429. The external device may include a computer, a multimedia device, a mobile computing device, etc. The I/O interface 429 may include wireline and/or wireless communication links.

[0101] The DVD control module 421 may receive data from the buffer 422, nonvolatile memory 423, the processor 424, the spindle/FM driver module 425, the analog front-end module 426, the write strategy module 427, the DSP module 428, and/or the I/O interface 429. The processor 424 may process the

data, including encoding, decoding, filtering, and/or formatting. The DSP module 428 performs signal processing, such as video and/or audio coding/decoding. The processed data may be output to the buffer 422, nonvolatile memory 423, the processor 424, the spindle/FM driver module 425, the analog front-end module 426, the write strategy module 427, the DSP module 428, and/or the I/O interface 429.

**[0102]** The DVD control module 421 may use the buffer 422 and/or nonvolatile memory 423 to store data related to the control and operation of the DVD drive 418. The buffer 422 may include DRAM, SDRAM, etc. The nonvolatile memory 423 may include flash memory (including NAND and NOR flash memory), phase change memory, magnetic RAM, or multi-state memory, in which each memory cell has more than two states. The DVD PCB 419 includes a power supply 430 that provides power to the components of the DVD drive 418.

**[0103]** The DVDA 420 may include a preamplifier device 431, a laser driver 432, and an optical device 433, which may be an optical read/write (ORW) device or an optical read-only (OR) device. A spindle motor 434 rotates an optical storage medium 435, and a feed motor 436 actuates the optical device 433 relative to the optical storage medium 435.

**[0104]** When reading data from the optical storage medium 435, the laser driver provides a read power to the optical device 433. The optical device 433 detects data from the optical storage medium 435, and transmits the data to the preamplifier device 431. The analog front-end module 426 receives data from the preamplifier device 431 and performs such functions as filtering and A/D conversion. To write to the optical storage medium 435, the write strategy module 427 transmits power level and timing information to the laser driver 432. The laser driver 432 controls the optical device 433 to write data to the optical storage medium 435.

**[0105]** Referring now to FIG. 16C, the teachings of the disclosure can be implemented in a transistors of a high definition television (HDTV) 437. The HDTV 437 includes a HDTV control module 438, a display 439, a power supply

440, memory 441, a storage device 442, a WLAN interface 443 and associated antenna 444, and an external interface 445.

**[0106]** The HDTV 437 can receive input signals from the WLAN interface 443 and/or the external interface 445, which sends and receives information via cable, broadband Internet, and/or satellite. The HDTV control module 438 may process the input signals, including encoding, decoding, filtering, and/or formatting, and generate output signals. The output signals may be communicated to one or more of the display 439, memory 441, the storage device 442, the WLAN interface 443, and the external interface 445.

**[0107]** Memory 441 may include random access memory (RAM) and/or nonvolatile memory such as flash memory, phase change memory, or multi-state memory, in which each memory cell has more than two states. The storage device 442 may include an optical storage drive, such as a DVD drive, and/or a hard disk drive (HDD). The HDTV control module 438 communicates externally via the WLAN interface 443 and/or the external interface 445. The power supply 440 provides power to the components of the HDTV 437.

**[0108]** Referring now to FIG. 16D, the teachings of the disclosure may be implemented in a transistors of a vehicle 446. The vehicle 446 may include a vehicle control system 447, a power supply 448, memory 449, a storage device 450, and a WLAN interface 452 and associated antenna 453. The vehicle control system 447 may be a powertrain control system, a body control system, an entertainment control system, an anti-lock braking system (ABS), a navigation system, a telematics system, a lane departure system, an adaptive cruise control system, etc.

**[0109]** The vehicle control system 447 may communicate with one or more sensors 454 and generate one or more output signals 456. The sensors 454 may include temperature sensors, acceleration sensors, pressure sensors, rotational sensors, airflow sensors, etc. The output signals 456 may control engine operating parameters, transmission operating parameters, suspension parameters, etc.

**[0110]** The power supply 448 provides power to the components of the vehicle 446. The vehicle control system 447 may store data in memory 449

and/or the storage device 450. Memory 449 may include random access memory (RAM) and/or nonvolatile memory such as flash memory, phase change memory, or multi-state memory, in which each memory cell has more than two states. The storage device 450 may include an optical storage drive, such as a DVD drive, and/or a hard disk drive (HDD). The vehicle control system 447 may communicate externally using the WLAN interface 452.

**[0111]** Referring now to FIG. 16E, the teachings of the disclosure can be implemented in a transistors of a cellular phone 458. The cellular phone 458 includes a phone control module 460, a power supply 462, memory 464, a storage device 466, and a cellular network interface 467. The cellular phone 458 may include a WLAN interface 468 and associated antenna 469, a microphone 470, an audio output 472 such as a speaker and/or output jack, a display 474, and a user input device 476 such as a keypad and/or pointing device.

**[0112]** The phone control module 460 may receive input signals from the cellular network interface 467, the WLAN interface 468, the microphone 470, and/or the user input device 476. The phone control module 460 may process signals, including encoding, decoding, filtering, and/or formatting, and generate output signals. The output signals may be communicated to one or more of memory 464, the storage device 466, the cellular network interface 467, the WLAN interface 468, and the audio output 472.

**[0113]** Memory 464 may include random access memory (RAM) and/or nonvolatile memory such as flash memory, phase change memory, or multi-state memory, in which each memory cell has more than two states. The storage device 466 may include an optical storage drive, such as a DVD drive, and/or a hard disk drive (HDD). The power supply 462 provides power to the components of the cellular phone 458.

**[0114]** Referring now to FIG. 16F, the teachings of the disclosure can be implemented in a transistors of a set top box 478. The set top box 478 includes a set top control module 480, a display 481, a power supply 482, memory 483, a storage device 484, and a WLAN interface 485 and associated antenna 486.

[0115] The set top control module 480 may receive input signals from the WLAN interface 485 and an external interface 487, which can send and receive information via cable, broadband Internet, and/or satellite. The set top control module 480 may process signals, including encoding, decoding, filtering, and/or formatting, and generate output signals. The output signals may include audio and/or video signals in standard and/or high definition formats. The output signals may be communicated to the WLAN interface 485 and/or to the display 481. The display 481 may include a television, a projector, and/or a monitor.

[0116] The power supply 482 provides power to the components of the set top box 478. Memory 483 may include random access memory (RAM) and/or nonvolatile memory such as flash memory, phase change memory, or multi-state memory, in which each memory cell has more than two states. The storage device 484 may include an optical storage drive, such as a DVD drive, and/or a hard disk drive (HDD).

[0117] Referring now to FIG. 16G, the teachings of the disclosure can be implemented in a transistors of a media player 489. The media player 489 may include a media player control module 490, a power supply 491, memory 492, a storage device 493, a WLAN interface 494 and associated antenna 495, and an external interface 499.

[0118] The media player control module 490 may receive input signals from the WLAN interface 494 and/or the external interface 499. The external interface 499 may include USB, infrared, and/or Ethernet. The input signals may include compressed audio and/or video, and may be compliant with the MP3 format. Additionally, the media player control module 490 may receive input from a user input 496 such as a keypad, touchpad, or individual buttons. The media player control module 490 may process input signals, including encoding, decoding, filtering, and/or formatting, and generate output signals.

[0119] The media player control module 490 may output audio signals to an audio output 497 and video signals to a display 498. The audio output 497 may include a speaker and/or an output jack. The display 498 may present a graphical user interface, which may include menus, icons, etc. The power supply 491 provides power to the components of the media player 489. Memory

492 may include random access memory (RAM) and/or nonvolatile memory such as flash memory, phase change memory, or multi-state memory, in which each memory cell has more than two states. The storage device 493 may include an optical storage drive, such as a DVD drive, and/or a hard disk drive (HDD).

**[0120]** Those skilled in the art can now appreciate from the foregoing description that the broad teachings of the present invention can be implemented in a variety of forms. Therefore, while this invention has been described in connection with particular examples thereof, the true scope of the invention should not be so limited since other modifications will become apparent to the skilled practitioner upon a study of the drawings, the specification and the following claims.

## CLAIMS

What is claimed is:

1. An integrated circuit comprising:

a first source;

a first drain;

a second source;

a first gate arranged between said first source and said first drain;

a second gate arranged between said first drain and said second source,

wherein said first and second gates define alternating first and second regions in said drain, wherein said first and second gates are arranged farther apart in said first regions than in said second regions; and

a well substrate contact arranged in said first regions.

2. An integrated circuit comprising:

a first source;

a first drain;

a second source;

a first gate arranged between said first source and said first drain;

a second gate arranged between said first drain and said second source,

wherein said first and second gates define alternating first and second regions in said drain, wherein said first and second gates are arranged farther apart in said first regions than in said second regions; and

R well substrate contacts arranged in said first regions, where R is an integer greater than one.

3. The integrated circuit of Claim 2 wherein R is an integer that is greater than three and less than seven.

4. The integrated circuit of Claim 1 wherein said integrated circuit includes a plurality of transistors.

5. The integrated circuit of Claim 4 wherein said transistors include PMOS transistors.

6. The integrated circuit of Claim 2 wherein said R well substrate contacts are associated with respective ones of R transistors.

7. An integrated circuit comprising:

a first source;

a first drain;

a second source;

a first gate arranged between said first source and said first drain;

a second gate arranged between said first drain and said second source,

wherein said first and second gates define alternating first and second regions in said drain, wherein said first and second gates are arranged farther apart in said first regions than in said second regions;

a second drain; and

a third gate arranged between said second source and said second drain,

wherein said second and third gates define alternating third and fourth regions, said second and third gates are arranged farther apart in said third regions than in said fourth regions,

wherein said first regions are arranged adjacent to said fourth regions and said second regions are arranged adjacent to said third regions, and

wherein said first and third regions include R well substrate contacts and R is an integer greater than one.

8. A method for providing an integrated circuit comprising:

providing a first source;

providing a first drain;

providing a second source;

locating a first gate between said first source and said first drain;

locating a second gate between said first drain and said second source;

defining alternating first and second regions in said drain using said first and second gates;

arranging said first and second gates farther apart in said first regions than in said second regions; and

locating a well substrate contact in said first regions.

9. A method for providing an integrated circuit comprising:

providing a first source;

providing a first drain;

providing a second source;

locating a first gate between said first source and said first drain;

locating a second gate between said first drain and said second source;

defining alternating first and second regions in said drain using said first and second gates;

arranging said first and second gates farther apart in said first regions than in said second regions; and

locating R well substrate contacts in said first regions, where R is an integer greater than one.

10. The method of Claim 9 wherein R is an integer that is greater than three and less than seven.

11. The method of Claim 8 wherein said integrated circuit includes a plurality of transistors.

12. The method of Claim 11 wherein said transistors include PMOS transistors.

13. The method of Claim 9 further comprising associating said R well substrate contacts with respective ones of R transistors.

14. A method for providing an integrated circuit comprising:

providing a first source;

providing a first drain;

providing a second source;

locating a first gate between said first source and said first drain;

locating a second gate between said first drain and said second source;

defining alternating first and second regions in said drain using said first and second gates;

arranging said first and second gates farther apart in said first regions than in said second regions;

providing a second drain;

providing a third gate between said second source and said second drain;

defining alternating third and fourth regions using said second and third gates;

arranging said second and third gates farther apart in said third regions than in said fourth regions; and

arranging said first regions adjacent to said fourth regions and said second regions adjacent to said third regions,

wherein said first and third regions include R well substrate contacts, where R is an integer greater than one.