Abstract.

The invention relates to a monolithic integrated semiconductor structure containing the following layer structure: A) a carrier layer based on doped or undoped Si, B) optionally a layer having the composition $B_xAl_yGa_zN_tP_v$, wherein x = 0 - 0.1, y = 0 - 1, z = 0 - 1, t = 0 - 0.1 and v = 0.9 - 1, C) a relaxation layer having the composition $B_xAl_yGa_zIn_uP_vSb_w$, wherein x = 0 - 0.1, y = 0 - 1, z = 0 - 1, u = 0 - 1, v = 0 - 1 and w = 0 - 1, wherein w and/or u is on the side facing toward layer A) or B) smaller than, equal to, or bigger than on the side facing away from layer A) or B) and wherein v = 1 - w and/or y = 1 - u - x - z, D) optionally a layer for blocking misfit dislocations and having the composition $B_xAl_yGa_zIn_uP_vSb_wN_t$, wherein x = 0 - 0.1, y = 0 - 1, z = 0 - 1, u = 0 - 1, v = 0 - 1, w = 0 - 1 and t = 0 - 0.1, E) optionally a layer for hetero-offset having the composition $B_xAl_yGa_zIn_uP_vSb_wN_tAs_r$, wherein x = 0 - 0.1, y = 0 - 1, z = 0 - 1, u = 0 - 1, v = 0 - 1, w = 0 - 1, t = 0 - 0.1 and r = 0 - 1, and F) an arbitrary, preferably group III/V, semiconductor material, or a combination of several different arbitrary semiconductor materials, wherein the sum of the above stoichiometric indices for all group III elements is always 1 and wherein the sum of the above stoichiometric indices for all group V elements is also always 1.