

CLAIMS

1. A module comprising:
 - a substrate having a plurality of contact regions; and
 - a spacer-chip assembly, in turn comprising:
 - at least first and second semiconductor dies, each having a plurality of electrical interconnect pillars and a plurality of contact pads;
 - a spacer wafer, said at least first and second semiconductor dies being secured to said spacer wafer, said spacer wafer including at least first and second semiconductor circuit features coupled to a first portion of said contact pads of said at least first and second semiconductor dies, said spacer wafer including wiring electrically coupling said at least first and second semiconductor dies via a second portion of said contact pads;
 - said spacer wafer having a plurality of holes formed therethrough, said plurality of electrical interconnect pillars extending through said holes and being secured to said contact regions on said substrate.
2. The module of Claim 1, wherein said semiconductor circuit features comprise decoupling capacitors.
3. The module of Claim 2, further comprising underfill disposed in said holes.
4. The module of Claim 3, further comprising over-mold between said at least first and second semiconductor dies.
5. The module of Claim 4, wherein said holes are sized to receive a single one of said pillars.
6. The module of Claim 4, wherein said holes are sized to receive multiple ones of said pillars.
7. The module of Claim 6, wherein said pillars comprise under bump metallurgy (UBM).
8. The module of any of claims 4 to 7, further comprising a glass-filled pocket formed in said spacer wafer, wherein:
 - at least a portion of said holes are formed in said glass;
 - said first semiconductor die comprises a silicon chip;
 - said second semiconductor die comprises a silicon carbide chip; and
 - those of said interconnect pillars associated with said silicon carbide chip extend into those of said holes in said glass.
9. The module of any of claims 4 to 8, wherein said plurality of electrical interconnect pillars are secured to

contact regions on said substrate via dippable paste.

10. The module of Claim 9, wherein said pillars comprise copper and said dippable paste comprises copper.
11. The module of Claim 9, wherein said pillars comprise copper and said dippable paste comprises lead-free solder.
12. The module of any of claims 4 to 11, wherein said plurality of electrical interconnect pillars are secured to contact regions on said substrate via controlled collapse chip connection (C4).
13. The module of any of claims 4 to 12, wherein said spacer wafer comprises glass and said decoupling capacitors comprise thin film capacitors.
14. The module of any of claims 4 to 13, wherein said spacer wafer comprises silicon and said decoupling capacitors are selected from the group consisting of deep trench capacitors and MIM (Metal-Insulator-Metal) capacitors.
15. A method comprising:
 - providing a spacer wafer, said spacer wafer having inner and outer surfaces, said spacer wafer including at least first and second semiconductor circuit features and wiring, adjacent said outer surface;
 - forming a plurality of trenches partially through said spacer wafer, spaced from said at least first and second semiconductor circuit features and said wiring;
 - providing first and second semiconductor dies, each having a plurality of electrical interconnect pillars and a plurality of contact pads, said electrical interconnect pillars having distal ends;
 - securing said first and second semiconductor dies to said spacer wafer via said plurality of contact pads with said interconnect pillars extending into said trenches, and with said contact pads coupled to said wiring and said semiconductor circuit features, to form a spacer-chip assembly;
 - processing said inner surface of said of said spacer wafer to open said trenches and expose said distal ends of said pillars;
 - applying electrically conductive connective material to said distal ends of said pillars; and
 - securing said spacer-chip assembly to a substrate via said electrically conductive connective material on said distal ends of said pillars.
16. The method of Claim 15, wherein applying said electrically conductive connective material comprises applying dippable paste.

17. The method of Claim 16, wherein said semiconductor circuit features comprise decoupling capacitors.
18. The method of Claim 17, further comprising applying underfill material into said trenches subsequent to said securing.
19. The method of Claim 18, further comprising applying over-molding over and between said first and second semiconductor dies after applying said underfill.
20. The method of Claim 19, further comprising processing said over-molding to render it flush with outer surfaces of said semiconductor dies.
21. The method of Claim 20, wherein:
said providing further comprises providing third and fourth semiconductor dies, each having a plurality of electrical interconnect pillars and a plurality of contact pads;
said securing further comprises securing said third and fourth semiconductor dies to said spacer wafer via said plurality of contact pads with said interconnect pillars extending into said trenches, and with said contact pads coupled to said wiring, to form said spacer-chip assembly;
further comprising singulating said spacer wafer to form a first module including said first and second semiconductor dies and a second module including said third and fourth semiconductor dies.
22. The method of Claim 21, further comprising partially dicing said spacer-chip assembly by forming cuts from outside into said spacer wafer, prior to processing said inner surface, wherein said processing of said inner surface of said spacer wafer effectuates said singulating via contacting said cuts.
23. The method of Claim 22, wherein said partial dicing comprises plasma dicing.
24. The method of any of claims 19 to 23, further comprising:
forming a pocket in said spacer wafer; and
adhering glass into said pocket;
wherein:
said forming of said plurality of trenches includes forming at least a portion of said trenches in said glass;
said first semiconductor die comprises a silicon chip;
said second semiconductor die comprises a silicon carbide chip; and
in said step of securing said first and second semiconductor dies to said spacer wafer via said plurality of contact pads with said interconnect pillars extending into said trenches, at least a portion of those of said interconnect pillars associated with said silicon carbide chip extend into those of said trenches in said glass.

25. The method of any of Claims 15 to 24, wherein applying said electrically conductive connective material comprises applying controlled collapse chip connection (C4) solder blobs.