FIG. 1

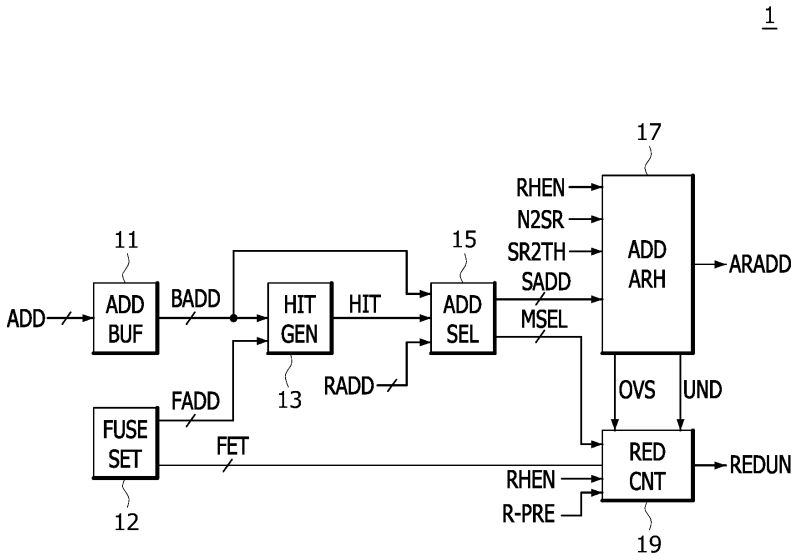

1
17
RHEN
N2SR
SR2TH
ADD
ARH
ARADD
11
15
ADD
BUF
BADD
HIT
GEN
HIT
ADD
SEL
SADD
MSEL
ADD
RADD
13
OVS
UND
FADD
FUSE
SET
FET
RED
CNT
REDUN
RHEN
R-PRE
12
19

FIG. 2

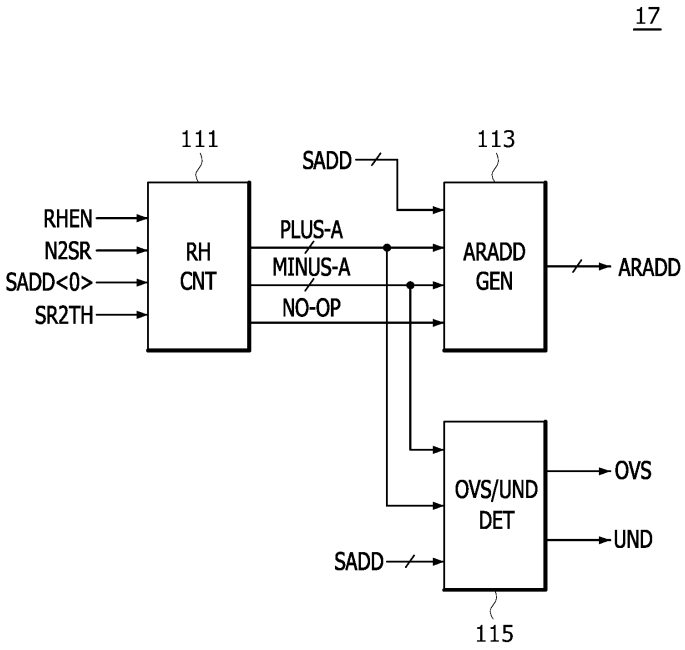

17
111
113
SADD
RHEN
N2SR
SADD<0>
SR2TH
RH
CNT
PLUS-A
MINUS-A
NO-OP
ARADD
GEN
ARADD
OVS/UND
DET
OVS
UND
SADD
115

FIG. 3

RHEN	N2SR	SADD<0>	SR2TH	N1/N2	1st/2nd	+/-
0	X	X	X	NO-OP = "H"		
1	0	0	0	N1	1st	+1
1	0	0	1	N1	2nd	-1
1	0	1	0	N1	1st	-1
1	0	1	1	N1	2nd	+1
1	1		0	N2	1st	+2
1	1		1	N2	2nd	-2
1	1		0	N2	1st	+2
1	1		1	N2	2nd	-2

FIG. 4

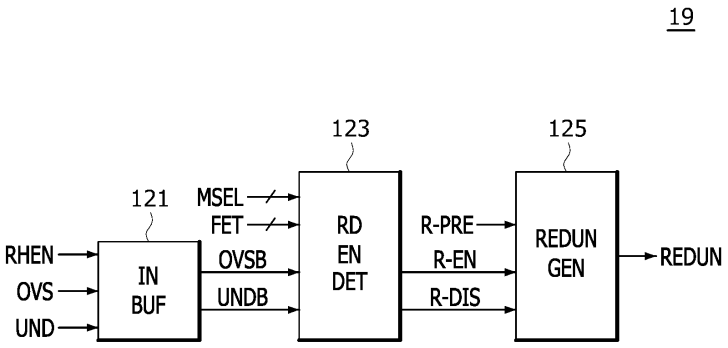

19
123
125
121
MSEL
FET
RD
EN
DET
R-PRE
R-EN
R-DIS
REDUN
GEN
REDUN
RHEN
OVS
UND
IN
BUF
OVSB
UNDB

FIG. 5

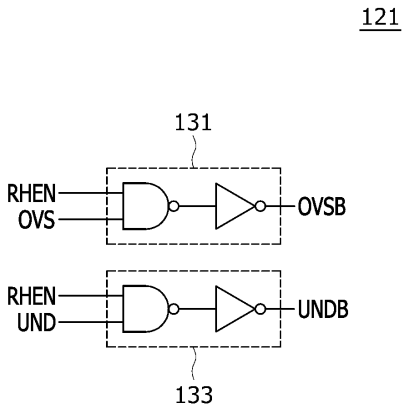


FIG. 6

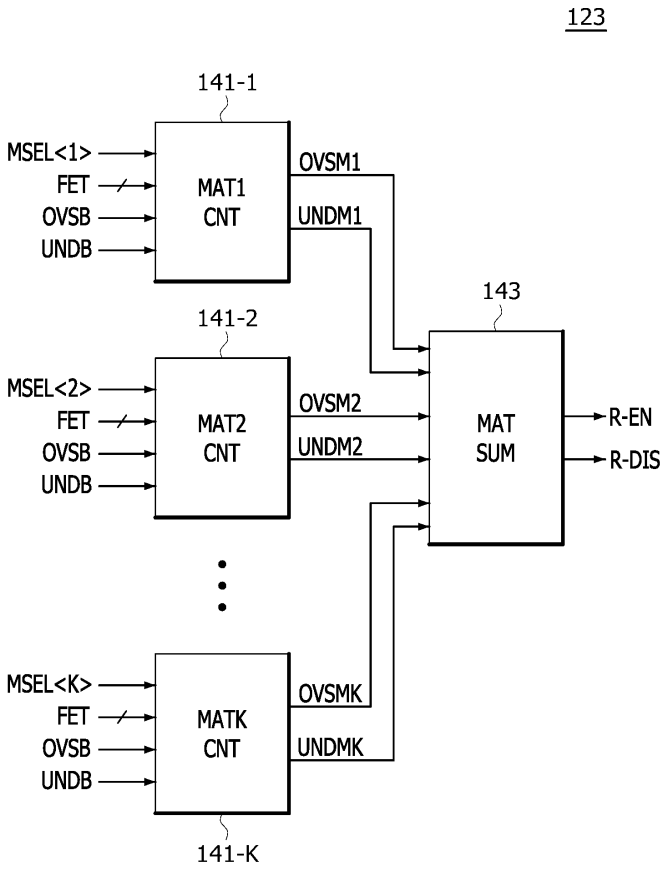

123
141-1
MSEL<1>
FET
OVSB
UNDB
MAT1
CNT
OVSM1
UNDM1
143
141-2
MSEL<2>
FET
OVSB
UNDB
MAT2
CNT
OVSM2
UNDM2
MAT
SUM
R-EN
R-DIS
MSEL<K>
FET
OVSB
UNDB
MATK
CNT
OVSMK
UNDMK
141-K

FIG. 7

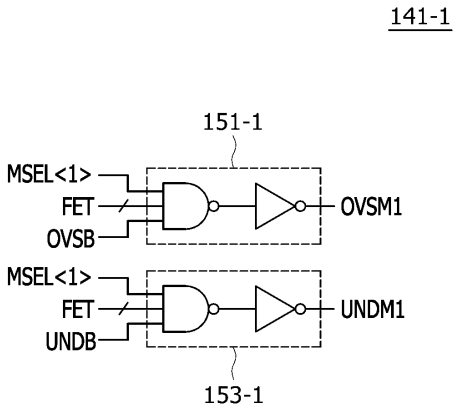


FIG. 8

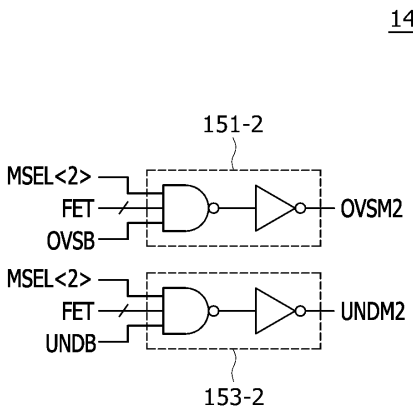


FIG. 9

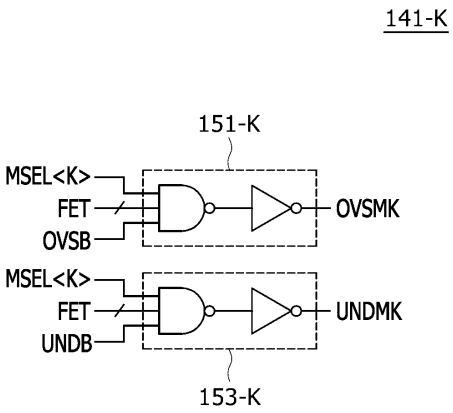


FIG. 10

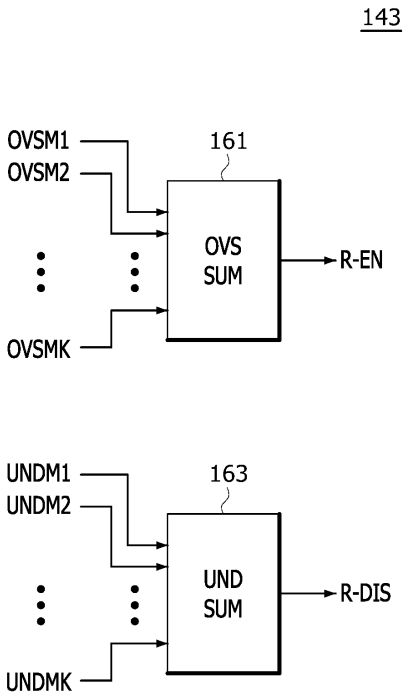

143
OVSM1
OVSM2
OVSMK
161
OVS
SUM
R-EN
UNDM1
UNDM2
UNDMK
163
UND
SUM
R-DIS

FIG. 11

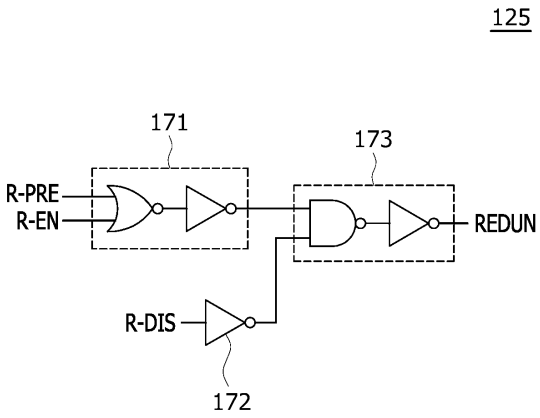


FIG. 12

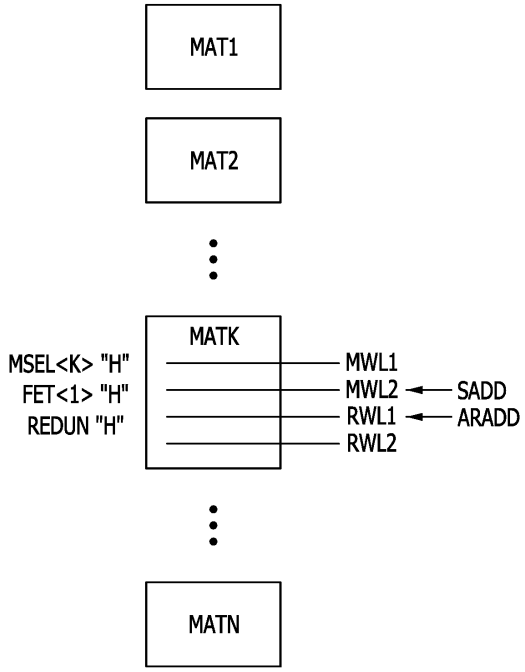

MAT1
MAT2
MATK
MSEL<K> "H"
FET<1> "H"
REDUN "H"
MWL1
MWL2
RWL1
RWL2
SADD
ARADD
MATN

FIG. 13

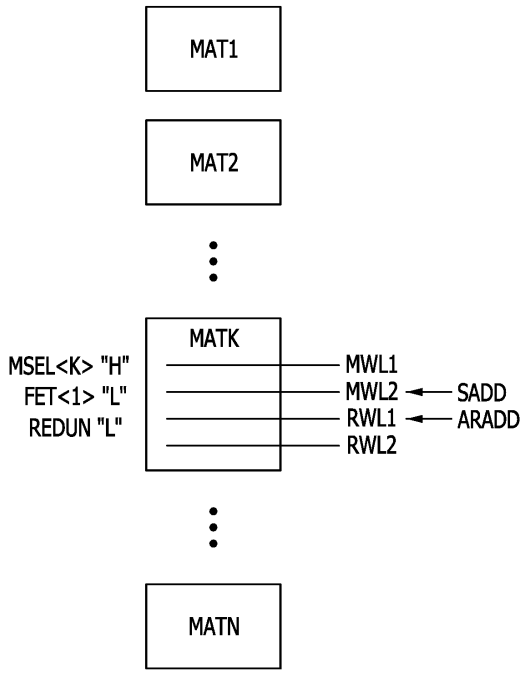

MAT1
MAT2
MATK
MSEL<K> "H"
FET<1> "L"
REDUN "L"
MWL1
MWL2
RWL1
RWL2
SADD
ARADD
MATN

FIG. 14

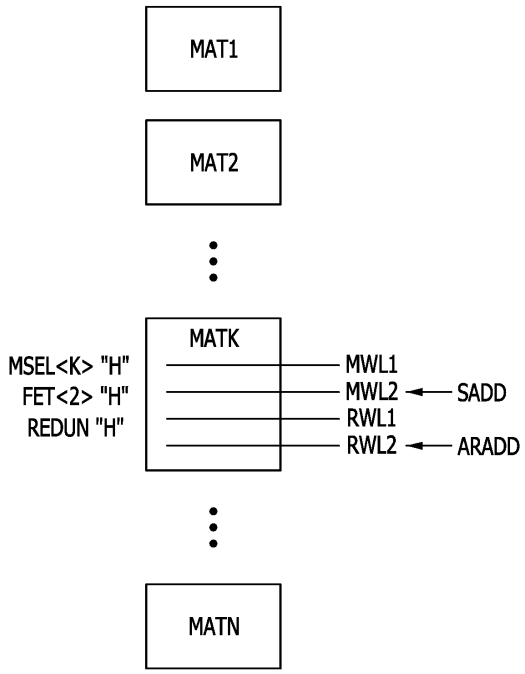

MAT1
MAT2
MATK
MSEL<K> "H"
FET<2> "H"
REDUN "H"
MWL1
MWL2
SADD
RWL1
RWL2
ARADD
MATN

FIG. 15

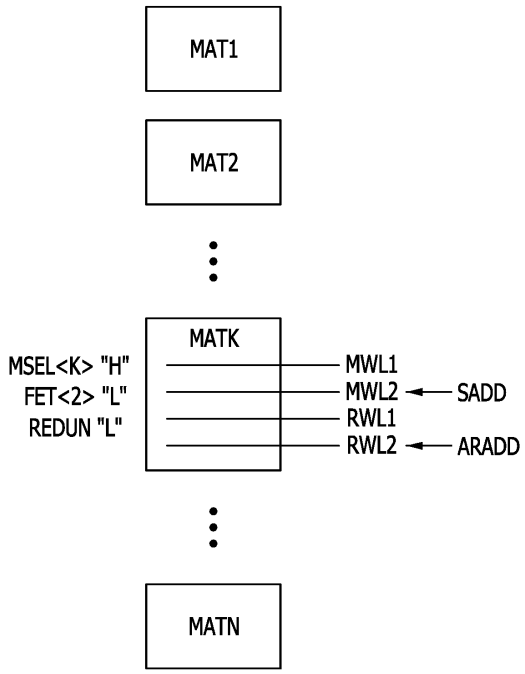

MAT1
MAT2
MATK
MSEL<K> "H"
FET<2> "L"
REDUN "L"
MWL1
MWL2
SADD
RWL1
RWL2
ARADD
MATN

FIG. 16

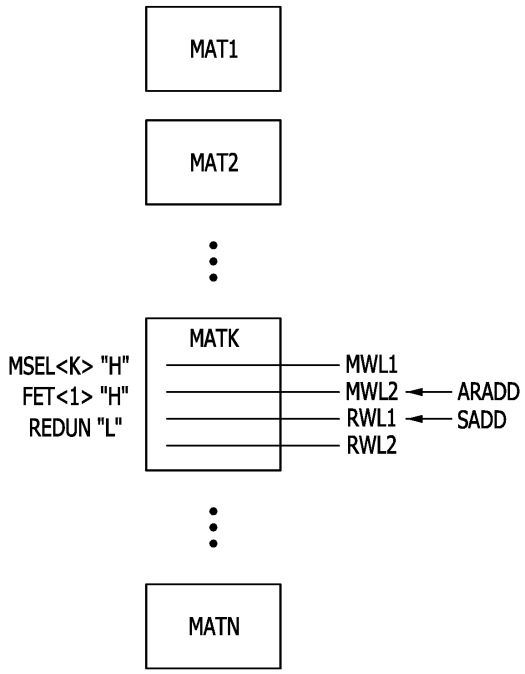

MAT1
MAT2
MATK
MSEL<K> "H"
FET<1> "H"
REDUN "L"
MWL1
MWL2
RWL1
RWL2
ARADD
SADD
MATN

FIG. 17

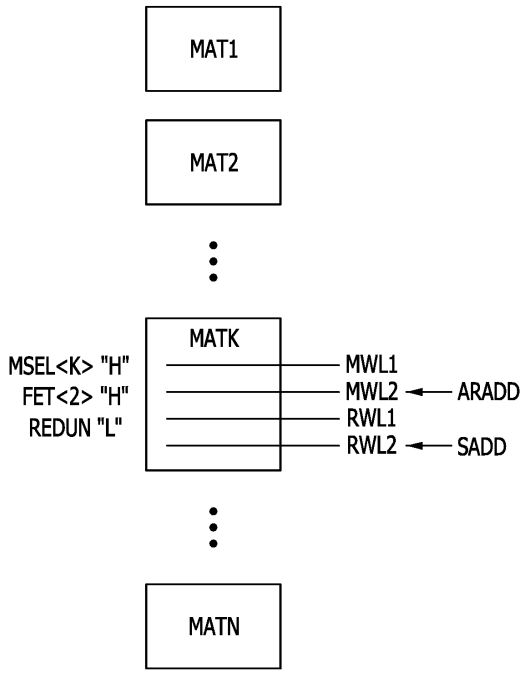
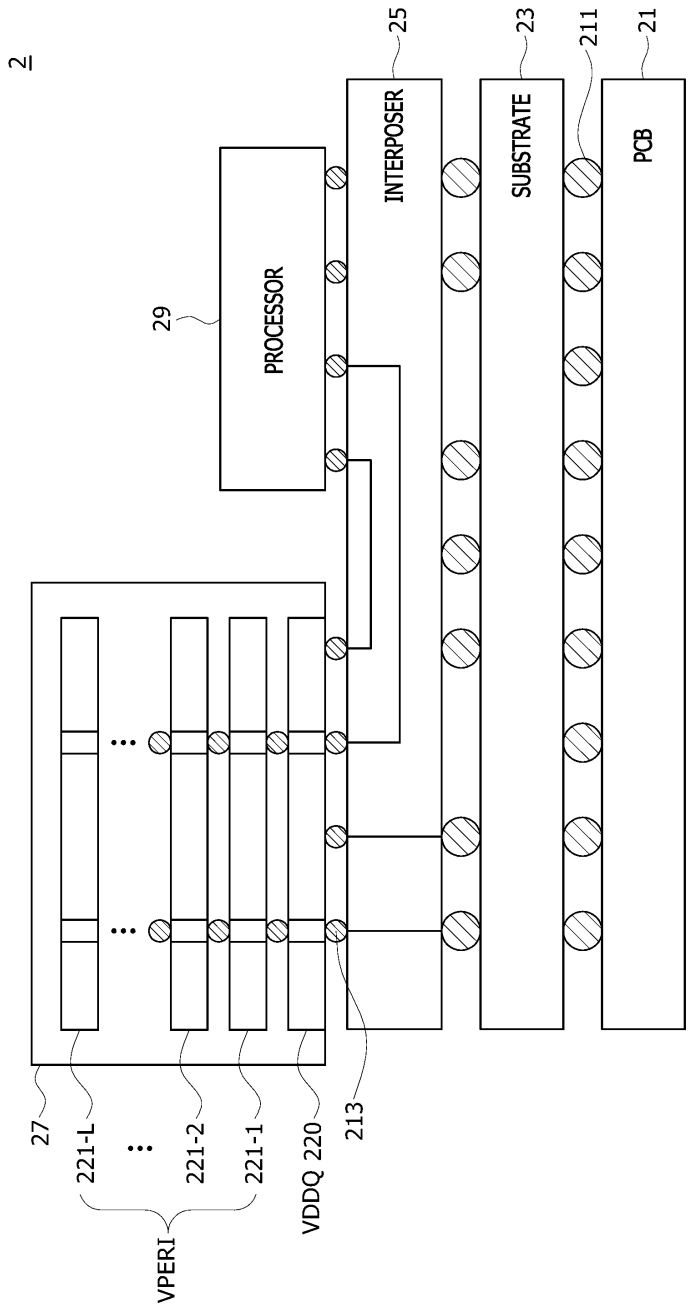

MAT1
MAT2
MATK
MSEL<K> "H"
FET<2> "H"
REDUN "L"
MWL1
MWL2
ARADD
RWL1
RWL2
SADD
MATN

FIG. 18


2
25
23
211
21
INTERPOSER
SUBSTRATE
PCB
29
PROCESSOR
27
221-L
221-2
221-1
VDDQ 220
213
VPERI