CLAIMS

What is claimed is:

1. A method comprising:

forming a non-planar transistor fin on a substrate;

forming a non-planar transistor gate over the non-planar transistor fin;

conformally depositing a dielectric material layer over the non-planar transistor gate and the non-planar transistor fin; and

substantially simultaneously forming non-planar transistor gate spacers from a portion of the dielectric material layer adjacent sidewalls of the non-planar transistor gate, and substantially simultaneously removing the dielectric material layer adjacent the non-planar transistor fin.

2. The method of claim 1, wherein substantially simultaneously forming non-planar transistor gate spacers from a portion of the dielectric material layer adjacent sidewalls of the non-planar transistor gate, and substantially simultaneously removing the dielectric material layer adjacent the non-planar transistor fin comprises:

forming a capping structure on a portion of the dielectric material layer proximate an upper portion of the non-planar transistor gate; and

directionally etching a portion of the dielectric material layer adjacent the non-planar transistor fin.

3. The method of claim 2, wherein forming the capping structure on the portion of the dielectric material layer comprises:

forming a sacrificial layer on the dielectric material layer;

recessing the sacrificial layer to expose a portion of the dielectric material layer;

altering the etching characteristics of the exposed portion of the dielectric material layer;

removing the sacrificial layer; and

removing the unaltered portion of the dielectric material layer.

4. The method of claim 3, wherein altering the etching characteristics of the exposed portion of the dielectric material layer comprises ion doping the exposed portion of the dielectric material layer.

5. The method of claim 4, further comprising annealing the ion doped portion of the dielectric material layer.

6. The method of claim 1, further comprising forming a source/drain structure adjacent the non-planar transistor gate.

7. The method of claim 6, wherein forming a source/drain structure comprising implanting a portion of the non-planar transistor fin with a dopant.

8. The method of claim 7, wherein implanting a portion of the non-planar transistor fin with a dopant comprises implanting the portion of the non-planar transistor fin with a P-type dopant.

9. The method of claim 7, wherein implanting a portion of the non-planar transistor fin with a dopant comprises implanting the portion of the non-planar transistor fin with an N-type dopant.

10. The method of claim 6, wherein forming a source/drain structure comprises removing a portion of the non-planar transistor fin and replacing the same with a source/drain structure.

11. The method of claim 10, wherein replacing the source/drain structure comprises epitaxially forming a silicon-containing source/drain structure.

12. A method comprising:

forming a non-planar transistor fin on a substrate;

forming a non-planar transistor gate over the non-planar transistor fin;

depositing a dielectric material layer over the non-planar transistor gate and the non-planar transistor fin;

forming non-planar transistor gate spacers from a portion of the dielectric material layer adjacent the non-planar transistor gate;

forming non-planar transistor fin spacers from a portion of the dielectric material layer adjacent the non-planar transistor gate;

removing at least a portion of the non-planar transistor fin from between the non-planar fins; and

removing the non-planar transistor fin spacers without removing the non-planar transistor fin spacers.

13. The method of claim 12, wherein forming non-planar transistor gate spacers and forming non-planar transistor fin spacers occurs substantially simultaneously.

14. The method of claim 12, wherein removing at least a portion of the non-planar transistor fin comprises etching at least a portion of the non-planar transistor fin.

15. The method of claim 12, wherein removing the non-planar transistor fin spacers comprises non-directionally etching interior and exterior surfaces of the non-planar transistor fin spacers.

16. The method of claim 12, further including forming a source/drain structure in place of the removed portion of the non-planar transistor fin.

17. The method of claim 16, wherein forming the source/drain structure comprises epitaxially forming a silicon-containing source/drain structure in place of the removed portion of the non-planar transistor fin.

18. A non-planar transistor, comprising:

at least one non-planar transistor fin,

at least one non-planar transistor gate formed over the at least one non-planar transistor fin, wherein the at least one non-planar transistor gate includes spacers adjacent thereto; and

at least one source/drain structure adjacent the at least one non-planar transistor gate, whererin the at least one source/drain structure lacks spacers adjacent thereto.

19. The non-planar transistor of claim 18, wherein the at least one source/drain structure comprises a portion of the at least one non-planar transistor fin having a dopant implanted therein.

20. The non-planar transistor of claim 19, wherein the portion of the at least one non-planar transistor having the dopant implanted therein comprises a portion of the non-planar transistor fin having a P-type dopant implanted therein.

21. The non-planar transistor of claim 19, wherein the portion of the at least one non-planar transistor having the dopant implanted therein comprises a portion of the non-planar transistor fin having an N-type dopant implanted therein.

22. The non-planar transistor of claim 18, wherein the source/drain structure comprises an epitaxially formed silicon-containing source/drain structure.

CLAIMS

What is claimed is:

1. A method comprising:

forming a non-planar transistor fin on a substrate;

forming a non-planar transistor gate over the non-planar transistor fin;

conformally depositing a dielectric material layer over the non-planar transistor gate and the non-planar transistor fin; and

forming non-planar transistor gate spacers from a portion of the dielectric material layer adjacent sidewalls of the non-planar transistor gate; and

removing the dielectric material layer adjacent the non-planar transistor fin;

wherein forming the non-planar transistor gate spacers and removing the dielectric material layer adjacent the non-planar transistor fin occur simultaneously;

wherein forming non-planar transistor gate spacers from a portion of the dielectric material layer adjacent sidewalls of the non-planar transistor gate, and removing the dielectric material layer adjacent the non-planar transistor fin comprises:

forming a capping structure on a portion of the dielectric material layer proximate an upper portion of the non-planar transistor gate, comprising:

forming a sacrificial layer on the dielectric material layer;

recessing the sacrificial layer to expose a portion of the dielectric material layer;

altering the etching characteristics of the exposed portion of the dielectric material layer;

removing the sacrificial layer; and

removing the unaltered portion of the dielectric material layer; and

directionally etching a portion of the dielectric material layer adjacent the non-planar transistor fin.

2. The method of claim 1, wherein altering the etching characteristics of the exposed portion of the dielectric material layer comprises ion doping the exposed portion of the dielectric material layer.

3. The method of claim 2, further comprising annealing the ion doped portion of the dielectric material layer.

4. The method of claim 1, further comprising forming a source/drain structure adjacent the non-planar transistor gate.

5. The method of claim 4, wherein forming a source/drain structure comprising implanting a portion of the non-planar transistor fin with a dopant.

6. The method of claim 5, wherein implanting a portion of the non-planar transistor fin with a dopant comprises implanting the portion of the non-planar transistor fin with a P-type dopant.

7. The method of claim 5, wherein implanting a portion of the non-planar transistor fin with a dopant comprises implanting the portion of the non-planar transistor fin with an N-type dopant.

8. The method of claim 4, wherein forming a source/drain structure comprises removing a portion of the non-planar transistor fin and replacing the same with a source/drain structure.

9. The method of claim 8, wherein replacing the source/drain structure comprises epitaxially forming a silicon-containing source/drain structure.