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Abstract

A bus-controlled signal processing system includes a serial data bus having first and second bus lines (SERBUS1,SERBUS2) for coupling various slave processors (160,150) to a master control processor (CONTROL μC). The slave devices require more than one data bus protocol. Each slave device has a bus clock terminal (CLOCK,SCL) and a bus data terminal (DATA,SDA). The slave devices dedicated to one protocol have their clock terminals connected to the first bus line and their data terminals connected to the second bus line. The slave devices dedicated to the other protocol have their data terminals connected to the first bus line and their clock terminals connected to the second bus line. The control processor changes the protocol being used to generate bus transmissions as required, and changes the function of the two bus lines when switching between bus protocols to prevent certain bus conflict conditions from occurring.

This Sheet Has Been Replaced

