HEAT DISSIPATION IN SEMICONDUCTOR ASSEMBLIES

The present invention relates to semiconductor assemblies which comprise an integrated circuit silicon chip.

The present invention relates particularly to semiconductor assemblies of the type which comprise a substrate formed from a dielectric material having an electrical circuit deposited thereon, a silicon chip, and a plurality of electrical leads connecting the electrical circuit and the silicon chip.

It is known that semiconductor assemblies with high density and high performance generate a substantial amount of heat in operation. For this reason microprocessors incorporating semiconductor assemblies generally have a built-in fan to cool down the semiconductor assemblies when the microprocessors are in operation. It is also known to include a means for dissipating heat from semiconductor assemblies. The known heat dissipation means comprises a metallic "plug", typically made from copper and having a plurality of fins, secured to the semiconductor assemblies. Typically, the plug is secured by means of a thermally conductive adhesive material to the silicon chips of the semiconductor assemblies. The plug acts as a primary thermal conductivity path for heat conduction so that heat is dissipated from the semiconductor assemblies.

One disadvantage of the known means of heat dissipation is that installation of the copper plug during construction of the semiconductor assemblies adds to the cost of the semiconductor assemblies.

In general terms, an object of the present invention is to provide a method of constructing a semi conductor assembly that includes an improved means of dissipating heat from the semiconductor assembly compared with the known heat dissipating means described in the preceding paragraph.

According to a first aspect of the present invention there is provided a method of constructing a semiconductor assembly which comprises an electrical circuit deposited on a substrate formed from a dielectric material and an integrated circuit silicon chip electrically connected to the electrical circuit, which method comprises the steps of:

(i) securing one of the silicon chip and a thermally conductive frame directly or indirectly to the substrate;

(ii) securing the other of the silicon chip and the frame directly or indirectly to the substrate so that the frame is positioned outboard of the silicon chip and defines a boundary around the silicon chip;

(iii) introducing an encapsulant to the space defined by the frame and the substrate; and

(iv) allowing said encapsulant to cure.

The frame has the dual purposes of dissipating heat from the assembly during use of the assembly and of defining a mould wall for retaining the encapsulant during construction of the assembly.

It is preferred that the frame be a parallelpiped.

The dielectric material may be any suitable material.

It is preferred that the dielectric material be a polyimide tape.

The electrical circuit may be deposited on one or both sides of the substrate.

The leads may be formed from any suitable material.

It is preferred that the leads be formed from a suitable low melting point material, such as gold, copper, copper plated with gold, nickel, tin and tin-lead alloy.

It is preferred that the semiconductor assembly comprises an electrical insulator material sandwiched between the substrate and the silicon chip.

The insulator material may be any suitable material.

It is preferred that the insulator material be an elastomer.

It is preferred that the frame and the silicon chip be secured to the elastomer material.

It is preferred that the elastomer material have adhesive properties.

According to a second aspect of the present invention there is provided a semiconductor assembly which comprises an integrated circuit silicon chip, an electrical circuit deposited on a substrate formed from a dielectric material, and electrical leads that electrically connect the silicon chip and the electrical circuit, the assembly being characterised in that it further comprises a thermally conductive frame secured directly or indirectly to the substrate and defining a boundary around the silicon chip.

According to a third aspect of the present invention there is also provided a structure for use in the construction of a semiconductor assembly, the structure comprising a thermally conductive frame as described above, a support framework spaced outwardly from the frame, and a plurality of tie-bars interconnecting the framework and the frame.

It is preferred that the tie-bars include stress-reducing means for reducing stress on the thermally conductive frame.

It is preferred that the assembly comprises a plurality of the thermally conductive frames positioned in an array interconnected by the tie-bars and bounded by the support framework.

The present invention is described further with reference to the accompanying drawings, of which:

Figure 1 is a vertical cross-section through a preferred embodiment of a semiconductor assembly in accordance with the present invention;

Figure 2 is a bottom plan view of the semiconductor assembly illustrated in Figure 1 with the silicon chip removed for clarity;

Figure 3 is a plan view of a preferred embodiment of a structure in accordance with the present invention for use in the construction of semiconductor assemblies; and

Figure 4 is a flow chart illustrating a preferred embodiment of a method of constructing a semiconductor assembly in accordance with the present invention.

With reference to Figures 1 and 2, a preferred embodiment of a semiconductor assembly in accordance with the present invention comprises:

(i) an electrical circuit (not shown) deposited on an upper surface of a tape 3 formed from a dielectric material, such as a polyimide;

(ii) a silicon chip 5, and

(iii)an electrical insulator material in the form of a pad 29 of an elastomer positioned between the tape 3 and the silicon chip 5.

The elastomer has adhesive properties and, as a consequence, the tape 3 and the silicon chip 5 adhere to the pad 29.

The electrical circuit on the tape 3 is connected to the silicon chip 5 by a plurality of leads extending from the upper surface of the tape 3. The leads 7 are connected to the silicon chip 5 in the manner described in a co-pending application entitled "Connecting Electrical Leads", the contents of which are incorporated herein by reference.

The semiconductor assembly further comprises a cover layer 16 of a protective material secured to the upper surface of the tape 3.

The semiconductor assembly further comprises 2 electrical connections 12 formed from an eutectic solder material.

The semiconductor assembly further comprises:

(i) a frame 8 formed from straight frame members connected together to form a square assembly; and

(ii) pads 37 of the same adhesive elastomer used to form the pad 29 positioned between the tape 3 and the frame 8 and thereby connecting the frame 8 indirectly to the underside of the tape 3.

The semiconductor assembly is completed by an encapsulant 9 which fills the space 10 between the silicon chip 5 and the frame 8.

The frame 8 has the dual purposes of dissipating heat generated in use of the semiconductor assembly and of defining a mould wall for the encapsulant 9 during construction of the semiconductor assembly.

A preferred embodiment of a method of constructing semiconductor assembly shown in Figures 1 and 2 is described with reference to Figure 4.

In a first step, a polyimide tape 3 with uBGA circuits thereon is provided and the pads 29 and 37 of elastomer are applied to the tape 3. As noted above, the elastomer is selected to have adhesive properties and the pads 29, 37 are secured to the tape 3 by virtue of these adhesive properties.

In a next step a thermally conductive frame 8 is applied to the pads 37 and is secured to the pads by virtue of the adhesive properties of the elastomer. The frame 8 has the square arrangement of frame members described above and 4 tie-bars 13, 14, 15, 16 which are described in more detail hereinafter.

In a next step the silicon chip 5 is positioned on the pad 29 and, due to the adhesive properties of the elastomer, adheres thereto. Thus, an arrangement is created wherein the frame 8 is disposed around and defines a boundary for the silicon chip 5.

An encapsulant is then dispensed inside the frame 8 and fills the space between the silicon chip 5 and the frame 8. The encapsulant is allowed to cure and so the assembly is completed.

Once completed, a cutter is used to cut the tie-bars 13, 14, 15, 16 from the frame 8.

Fig. 3 illustrates a structure 18 for use in the construction of a plurality of the semiconductor assemblies shown in Figures 1 and 2.

The structure 18 comprises a plurality of frames designated 8(a), 8(b), 8(c), 8(d), 8(e), etc connected via tie bars 13, 14, 15, 16 to a support framework 19. Considering frame 8(a), the tie-bars 13, 16 are connected to the framework 19, and the tie-bars 14 and 15 are connected to the adjacent frames 8(d) and 8(b). The framework 19 also comprises a number of pin-holes 20 which allow the structure to be secured to a support. Thus, in the arrangement shown a total of 18 semiconductor assemblies can be supported by the structure 18 during construction. Each of the tie-bars 13, 14, 15, 16 is in the form of a stepped structure with a series of straight sections 21, 22, 23, 24, 25 to minimise the risk of a thermal distortion of the frames 8 during construction of the semiconductor assemblies.

Many modifications may be made to the preferred embodiment of the present invention described above without departing from the spirit and scope of the present invention.

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THE CLAIMS DEFINING THE INVENTION ARE AS FOLLOWS:

1. A method of constructing a semiconductor assembly which comprises an electrical circuit deposited on a substrate formed from a dielectric material and an integrated circuit silicon chip electrically connected to the electrical circuit, which method comprises the steps of:

(i) securing one of the silicon chip and a thermally conductive frame directly or indirectly to the substrate;

(ii) securing the other of the silicon chip and the frame directly or indirectly to the substrate so that the frame is positioned outboard of the silicon chip and defines a boundary around the silicon chip;

(iii) introducing an encapsulant to the space defined by the frame and the substrate; and

(iv) allowing said encapsulant to cure.

2. The method defined in claim 1, wherein steps (i) and (ii) comprises securing an electrical insulator to the substrate and, thereafter, securing the frame and the silicon chip to the insulator.

3. The method defined in claim 2 wherein the electrical insulator is an elastomer having adhesive properties.

4. The method defined in any one of the preceding claims wherein the dielectric material is a polyimide and the substrate is in the form of a tape.

5. A semiconductor assembly which comprises an integrated circuit silicon chip, an electrical current deposited on a substrate formed from a dielectric material, and electrical leads that electrically connect the silicon chip and the electrical circuit, the assembly being characterised in that it further comprises a thermally conductive frame secured directly or indirectly to the substrate and defines a boundary around the silicon chip.

6. A structure for use in the construction of a semiconductor assembly, the structure comprising a thermally conductive frame as defined in any one of the preceding

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claims, a support framework spaced outwardly from the frame, and a plurality of tie-bars interconnecting the framework and the frame.

7. The structure defined in claim 6, wherein the tie-bars comprise a stress-reducing means for reducing stress on the frame.

8. The structure defined in claim 6 or claim 7 comprises a plurality of the frames positioned in an array interconnected by tie-bars and bounded by the support framework.