

PATENT SPECIFICATION

(11) 1375 802

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- (21) Application No. 5950/73 (22) Filed 7 Feb. 1973
(31) Convention Application No. 244475 (32) Filed 17 April 1972 in
(33) United States of America (US)
(44) Complete Specification published 27 Nov. 1974
(51) International Classification H03K 3/00
(52) Index at acceptance

H3T 1C2 1PX 2A1S 2B2 2B4 2B6 2E 2J 2T2Z 2T3J 3D
3F1 3J 4C 4D 4E1N 4E2N 4G 5E



(54) LOGIC PULSE SOURCE

(71) We, HEWLETT - PACKARD COMPANY, of 1501 Page Mill Road, Palo Alto, California, United States of America, a corporation organized and existing under the laws of the State of California, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

The invention is concerned with improvements in or relating to logic pulse sources.

In contrast to analog circuitry wherein test signals may be conveniently introduced at selected circuit nodes, digital circuitry commonly presents test conditions which prevent injection of test signals at selected circuit nodes. For example, in testing a cascaded series of gates, the gate input desired to be tested may be directly coupled to the output of a preceding gate which, if operating in the low state, may clamp the test input and prevent effective injection of a test pulse by ordinary means at that circuit node. The common solution to this problem involves disconnecting the test input from the preceding output so that the input state may be electrically unclamped and suitably tested. However, circuit nodes frequently cannot be isolated without altering bias or other operating conditions.

It is an object of the present invention to provide an improved logic pulse source.

The present invention provides a logic pulse source comprising: a pair of output signal stages connected to a common output, each of the output signal stages being normally operable in a non-conductive signal condition which presents a high output impedance, and in conductive signal condition for conducting signal current with respect to said common output in opposite conduction directions during operation of each of the output signal stages in their respective conductive signal conditions; circuit means connected to apply to said output signal stages a sequence of an initial and a subsequent

timing pulse in response to a trigger signal applied to said circuit means, the trailing edge of the initial timing pulse and leading edge of the subsequent timing pulse being substantially coincident for sequentially operating each of said output signal stages in the respective conductive signal condition; and actuating means for producing said sequence of timing pulses.

Preferably said circuit means includes a pair of amplifier circuits each of which operates on signals applied thereto above a selected threshold level; first differentiator means connected to apply said trigger signals to one of said amplifier circuits, and second differentiator means connected to apply an output signal from said one amplifier circuit to the other of said amplifier circuits for producing at the output of the second amplifier circuit a timing pulse having a leading edge substantially coincident with the trailing edge of the output signal from the first amplifier circuit; and means coupled to the output of the first one of said amplifier circuits for producing another timing pulse having a leading edge substantially coincident with the leading edge of the output signal from the first amplifier circuit.

Preferably said actuating means includes a bistable circuit for supplying said trigger signals in response to signal applied to the input of the bistable circuit; and a manually-actuated switch connected to the input of said bistable circuit for selectively altering the operating condition thereof to produce said trigger signals.

There now follows a detailed description to be read with reference to the accompanying drawing of a logic pulse source according to the invention; it is to be clearly understood that the logic pulse source has been selected for description to illustrate the invention by way of example.

Referring now to the drawing which is a schematic diagram of a logic source according to the present invention, a manually-operated single-pole, double-throw switch 9 is connected between ground and a selected one of

the inputs of a pair of cross-connected inverting amplifiers 11 and 13. This circuit arrangement produces a single-step output at 15 (independently of contact bounce of the switch 9) which is then differentiated by a differentiator provided by a resistance-capacitance circuit 17. The resulting differentiated pulse is applied to an inverter amplifier 19 which produces an output pulse at an output 21, the pulse '21' having pulse width ($t_0 \rightarrow t_1$) equal to the time period that the differentiated pulse at the output 15 remains above the operating threshold voltage v of the amplifier 19.

The pulse 21 is applied through cascaded inverter amplifiers 23 and 25 and a lead network 27 to one input 29 of the output stage and through a differentiator 31 and an inverter amplifier 33 (similar to the differentiator 17 and the inverter amplifier 19) and a resistor 34 to another input 35 of the output stage. The differentiator 31 produces a pulse of the same polarity as the pulse applied to the input of amplifier 19 in response to the trailing edge of the pulse 21 from the amplifier 19, and this causes the amplifier 33 to produce a pulse having a pulse width ($t_1 \rightarrow t_2$) equal to the time period that the differentiated pulse applied to the input of the amplifier 33 remains above the operating threshold voltage v of this amplifier. The signals thus arrive at the inputs 29 and 35 of the output stage delayed in time but with common polarity for initial operation of the switch 9. Pulses of inverted sign formed by return operation of the switch 9 are not passed by the amplifiers 19 and 33. The amplifiers 11, 13, 19, 23, 25 and 33 may all be formed in one or more integrated circuits of conventional designs and may be biased from supply buses, as later described.

The output stage includes a pair of input transistors 37 and 39 which have base electrodes connected to receive the pulses on leads 35 and 29 respectively and which are biased via a resistor 41 and collector loads 43 and 45 respectively to be normally non-conductive in the absence of the applied pulses. Output transistors 47 and 49 have base electrodes connected to receive the respective ones of the collector loads and have collector-emitter output circuits that are serially connected through the resistor 41 to the supply bus 59. In this arrangement, the output transistors 47 and 49 are normally non-conductive and an output node 51 at the common connection of the transistor output circuits thus presents a high output impedance of the order of 1,000 kilohms. This "off" operating condition is ideally suited for probing nodes of a circuit under test because the high impedance thus presented does not load down the circuit node under test. The pulses at 29 and 35 that are produced in the manner described in response to manual activation of the switch 9 cause the transistors 39 and 49 to become

conductive momentarily followed in sequence by momentary conduction of the transistors 37 and 47. These two operating conditions cause the output node 51 to be clamped momentarily ($t_0 \rightarrow t_1$) at ground potential (or "low" state) and then, in sequence, clamped momentarily ($t_1 \rightarrow t_2$) at about the bus potential (or "high" state). After termination of the pulse 35 applied to the transistor 37, the output node 51 is again in the "off" condition of high output impedance. If node under test is initially in the logic "low" state, the first pulse ($t_0 \rightarrow t_1$) from the transistor 49 will have substantially no effect, while the following pulse ($t_1 \rightarrow t_2$) from the transistor 47 will effect a state change at the node under test. Similarly, if the node under test is initially in the logic "high" state, then the first pulse ($t_0 \rightarrow t_1$) will effect a change at the node to a logic "low" state by clamping the node to ground momentarily through the transistor 49. The subsequent pulse ($t_1 \rightarrow t_2$) thus drives the node under test to the "high" state again. This has the effect of being able to alter any logic state of a circuit node under test simply by actuating the switch 9.

In order to insure adequate drive current to alter the logic state of a circuit node under test, the output circuit includes a large capacitor 53 which serves as a source of charge for momentary delivery to the output when the transistor 47 is rendered momentarily conductive. This capacitor, which is charged slowly at low initial current levels from the supply bus discharges through a parallel-connected resistor 55 and capacitor 57 into the circuit node under test for about 400 nanoseconds with a peak current of approximately one ampere. This results in extremely low average power dissipation in a component connected to a circuit node under test. The danger of accidental damage to test circuits is thus extremely remote. The resistor 55 and the capacitor 51 limit the current to safe values in case of inadvertent connection of the output to high voltages.

No pulses reach the transistors 37 and 39 upon return of the switch 9 to its normal contact position, and these transistors 37, 39 are returned to the non-conductive state approximately 800 nanoseconds after the initial activation of the switch 9.

A supply bus 59 connected to the resistor 41 may be connected to receive power (at +5volts) from the circuit under test and the amplifiers 11, 13, 19, 25 and 33 (in integrated circuit form) are connected to receive bias signal from the supply bus 59 through a forward-conducting germanium diode 61. This provides a few tenths volt drop for bias of the transistors 37, 39 relative to their respective drive amplifiers 25, 33 and provides back-bias protection against inadvertent reversal of polarity in connecting the supply bus to a source of voltage. A Zener diode 63

is connected to limit the bias signal for the amplifiers to a safe maximum value.

WHAT WE CLAIM IS:—

5 1. A logic pulse source comprising a pair of output signal stages connected to a common output, each of the output signal stages being normally operable in a non-conductive signal condition which presents a high output impedance, and in conductive signal condition for conducting signal current with respect to said common output in opposite conduction directions during operation of each of the output signal stages in their respective conductive signal conditions; circuit means connected to apply to said output signal stages a sequence of an initial and a subsequent timing pulse in response to a trigger signal applied to said circuit means, the trailing edge of the initial timing pulse and leading edge of the subsequent timing pulse being substantially coincident for sequentially operating each of said output signal stages in the respective conductive signal condition; and actuating means for selectively applying trigger signals to said circuit means for producing said sequence of timing pulses.

2. A logic pulse source according to claim 1 wherein said circuit means includes a pair of amplifier circuits each of which operates on signals applied thereto above a selected threshold level; first differentiator means connected to apply said trigger signals to one of

said amplifier circuits, and second differentiator means connected to apply an output signal from said one amplifier circuit to the other of said amplifier circuits for producing at the output of the second amplifier circuit a timing pulse having a leading edge substantially coincident with the trailing edge of the output signal from the first amplifier circuit; and means coupled to the output of the first one of said amplifier circuits for producing another timing pulse having a leading edge substantially coincident with the leading edge of the output signal from the first amplifier circuit.

3. A logic pulse source according to either one of claims 1 and 2 wherein said actuating means includes a bistable circuit for supplying said trigger signals in response to signal applied to the input of the bistable circuit; and a manually-actuated switch connected to the input of said bistable circuit for selectively altering the operating condition thereof to produce said trigger signals.

4. A logic pulse source according to claim 1 substantially as hereinbefore described with reference to the accompanying drawing.

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is connected to limit the bias signal for the amplifiers to a safe maximum value.

WHAT WE CLAIM IS:—

1. A logic pulse source comprising a pair
5 of output signal stages connected to a common
output, each of the output signal stages being
normally operable in a non-conductive signal
condition which presents a high output
10 impedance, and in conductive signal condi-
tion for conducting signal current with respect
to said common output in opposite con-
duction directions during operation of each
of the output signal stages in their respective
15 conductive signal conditions; circuit means
connected to apply to said output signal
stages a sequence of an initial and a sub-
sequent timing pulse in response to a trigger
signal applied to said circuit means, the trail-
20 ing edge of the initial timing pulse and lead-
ing edge of the subsequent timing pulse being
substantially coincident for sequentially
operating each of said output signal stages in
the respective conductive signal condition;
25 and actuating means for selectively applying
trigger signals to said circuit means for pro-
ducing said sequence of timing pulses.

2. A logic pulse source according to claim 1
wherein said circuit means includes a pair of
30 amplifier circuits each of which operates on
signals applied thereto above a selected thresh-
old level; first differentiator means con-
nected to apply said trigger signals to one of

said amplifier circuits, and second differen-
tiator means connected to apply an output
signal from said one amplifier circuit to the
other of said amplifier circuits for producing
35 at the output of the second amplifier circuit a
timing pulse having a leading edge substan-
tially coincident with the trailing edge of
the output signal from the first amplifier cir-
40 cuit; and means coupled to the output of the
first one of said amplifier circuits for produc-
ing another timing pulse having a leading
edge substantially coincident with the leading
45 edge of the output signal from the first ampli-
fier circuit.

3. A logic pulse source according to either
one of claims 1 and 2 wherein said actuating
means includes a bistable circuit for supply-
50 ing said trigger signals in response to signal
applied to the input of the bistable circuit;
and a manually-actuated switch connected to
the input of said bistable circuit for selectively
altering the operating condition thereof to
55 produce said trigger signals.

4. A logic pulse source according to claim
1 substantially as hereinbefore described with
reference to the accompanying drawing.

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