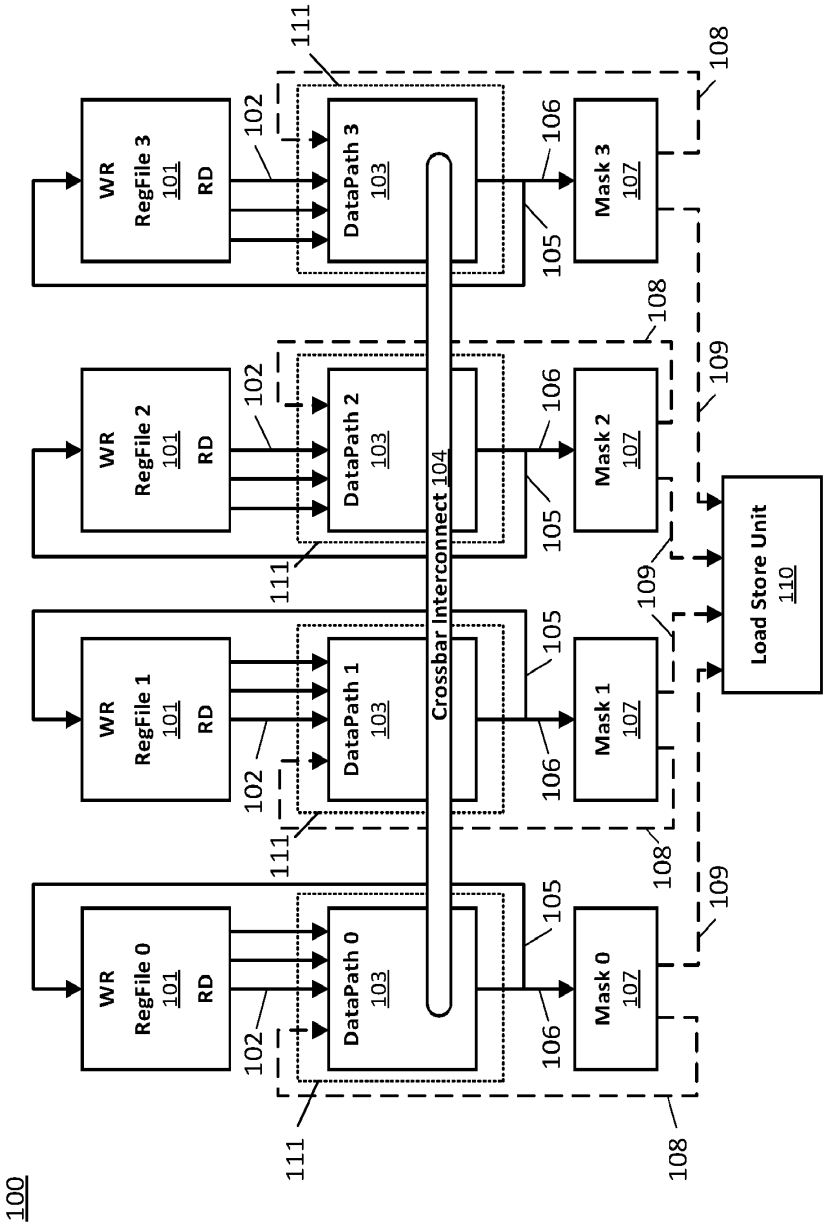
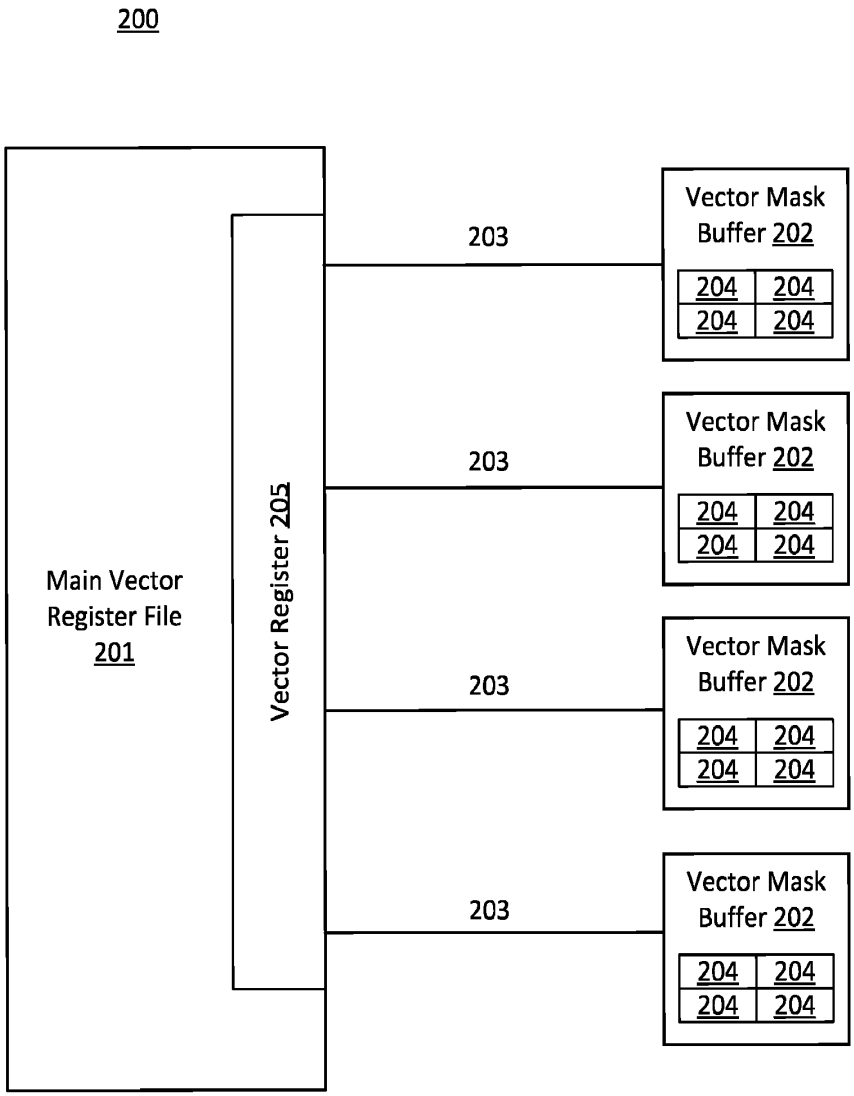

100
WR RegFile 3 101 RD
WR RegFile 2 101 RD
WR RegFile 1 101 RD
WR RegFile 0 101 RD
DataPath 3 103
DataPath 2 103
DataPath 1 103
DataPath 0 103
Crossbar Interconnect 104
Mask 3 107
Mask 2 107
Mask 1 107
Mask 0 107
Load Store Unit 110
102
105
106
108
109
111

FIG. 1

FIG. 2


200
Main Vector Register File 201
Vector Register 205
203
203
203
203
Vector Mask Buffer 202
204
Vector Mask Buffer 202
204
Vector Mask Buffer 202
204
Vector Mask Buffer 202
204

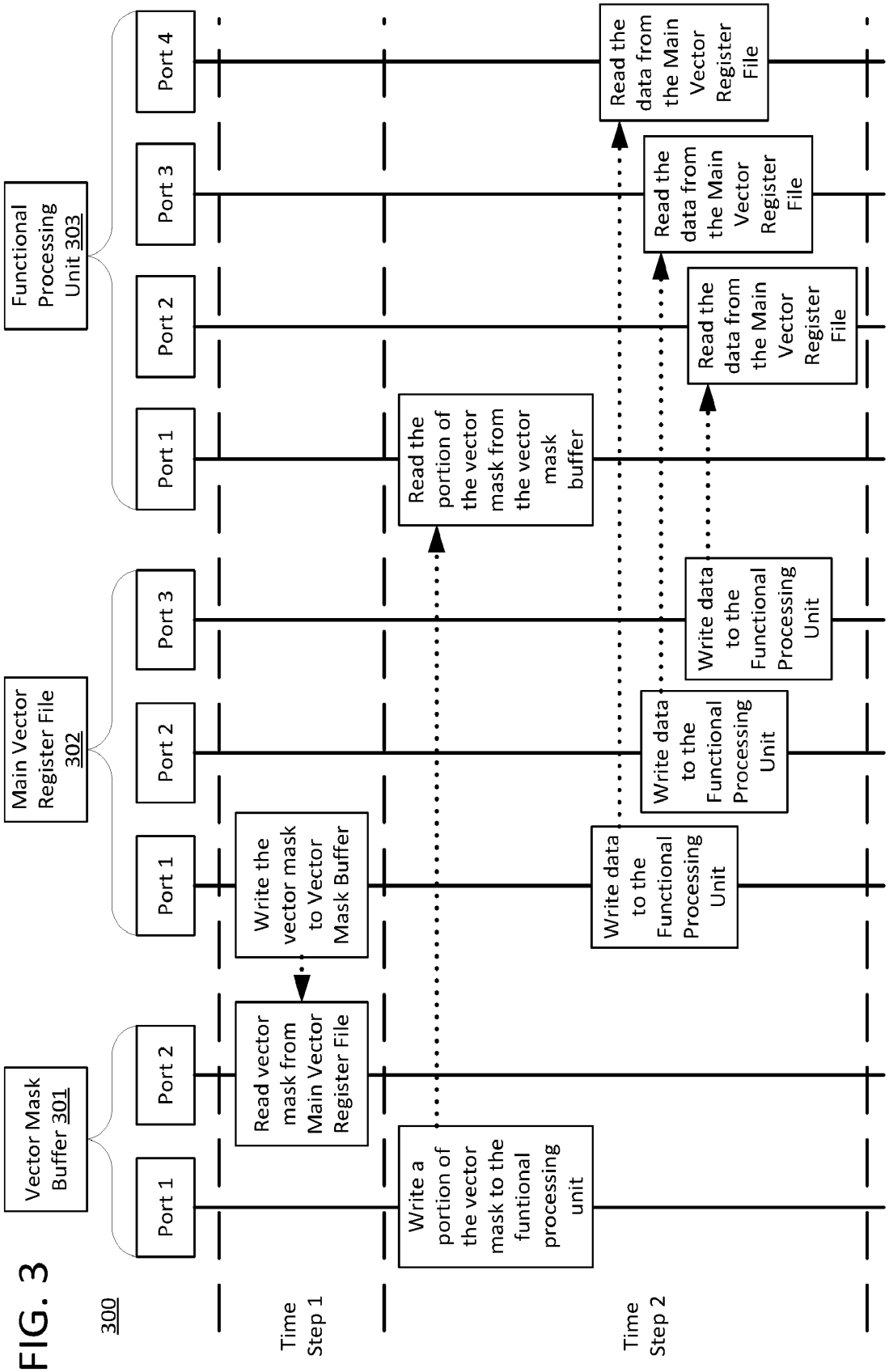
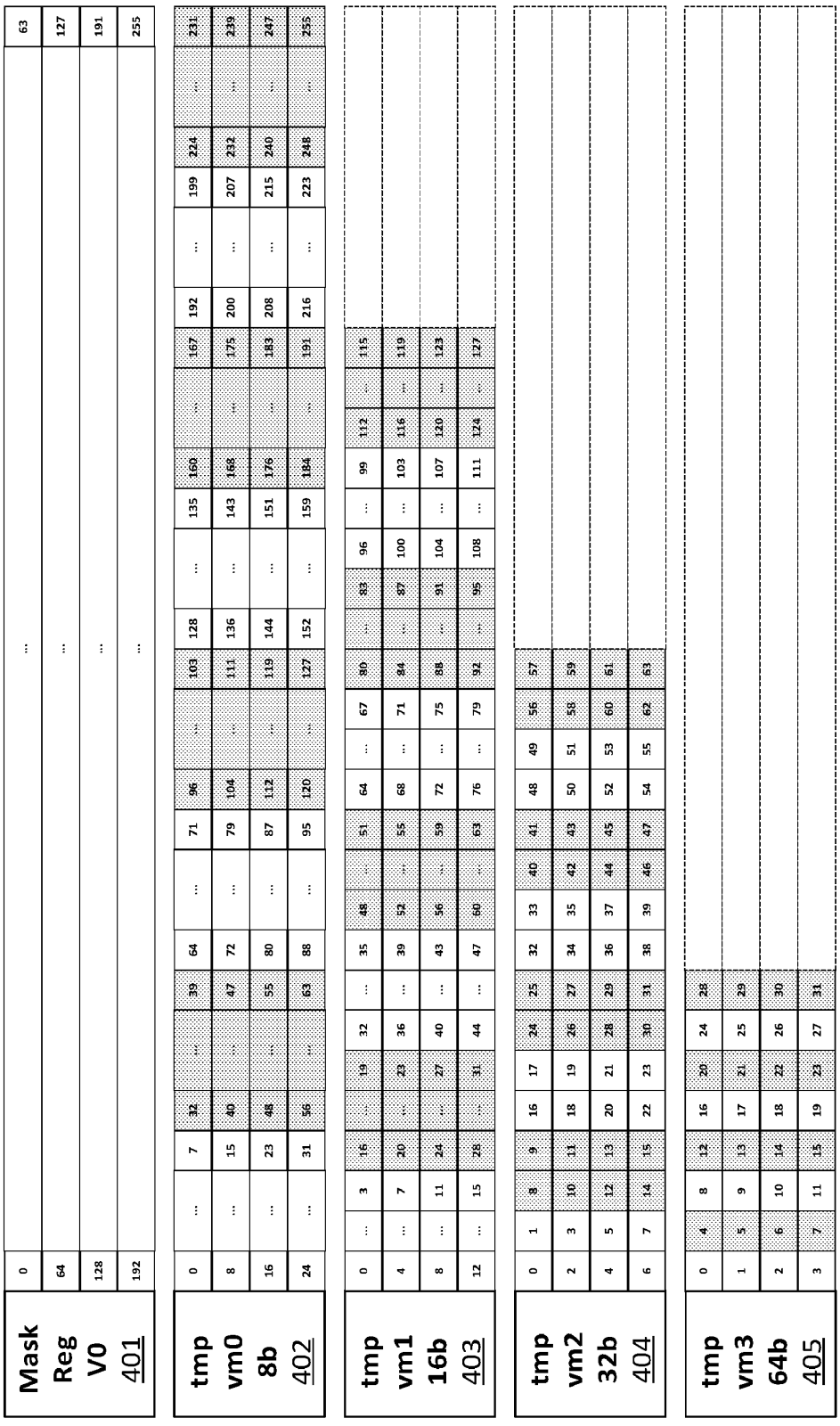

300
Vector Mask Buffer 301
Port 1
Port 2
Main Vector Register File 302
Port 1
Port 2
Port 3
Functional Processing Unit 303
Port 1
Port 2
Port 3
Port 4
Time Step 1
Time Step 2
Write a portion of the vector mask to the funtional processing unit
Read vector mask from Main Vector Register File
Write the vector mask to Vector Mask Buffer
Read the portion of the vector mask from the vector mask buffer
Write data to the Functional Processing Unit
Write data to the Functional Processing Unit
Write data to the Functional Processing Unit
Read the data from the Main Vector Register File
Read the data from the Main Vector Register File
Read the data from the Main Vector Register File

FIG. 3

FIG. 4


400
Mask Reg V0 401
tmp vm0 8b 402
tmp vm1 16b 403
tmp vm2 32b 404
tmp vm3 64b 405
lane0
lane1
lane2
lane3

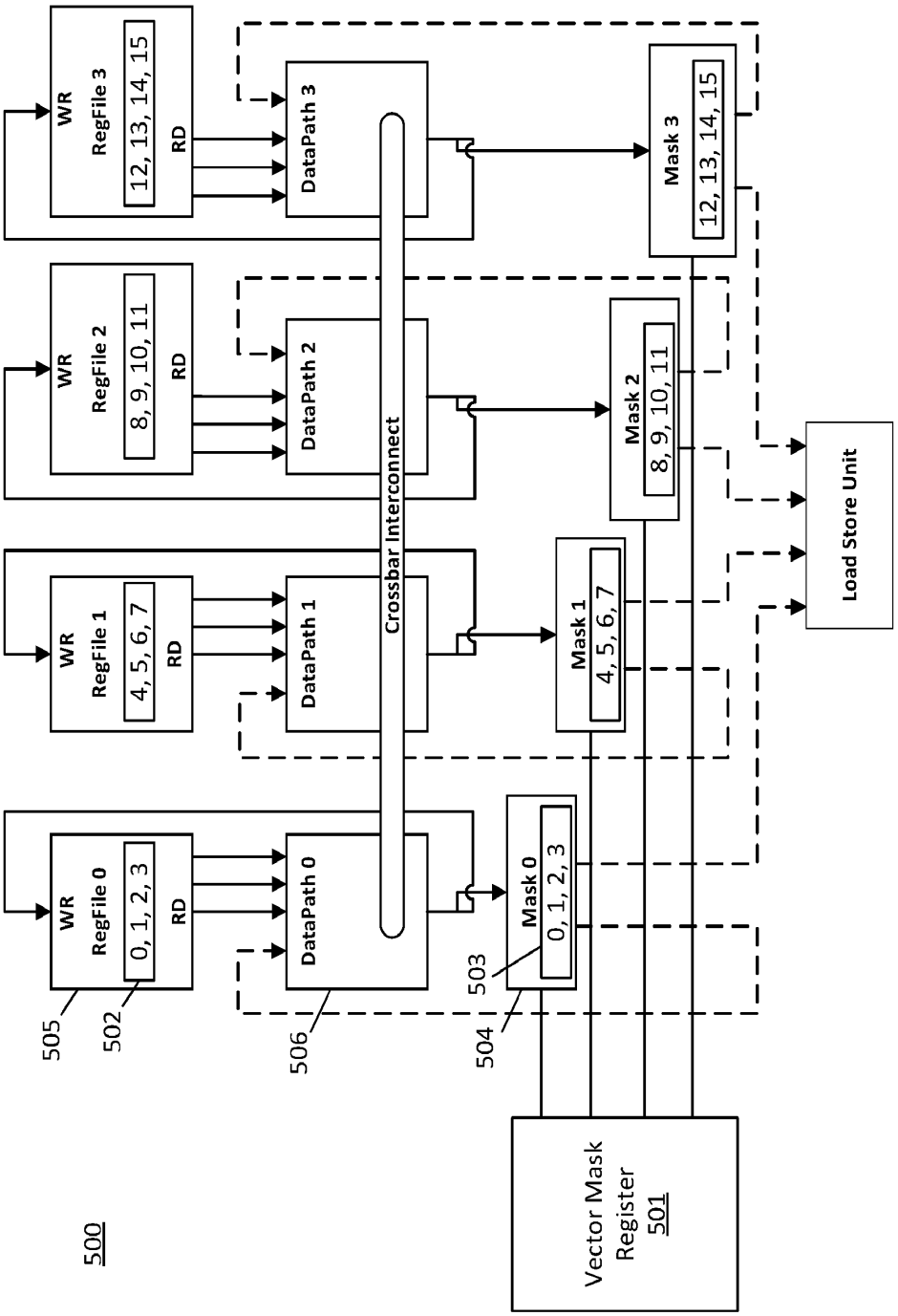

WR
RegFile 3
12, 13, 14, 15
RD
DataPath 3
Mask 3
12, 13, 14, 15
WR
RegFile 2
8, 9, 10, 11
RD
DataPath 2
Mask 2
8, 9, 10, 11
Crossbar Interconnect
WR
RegFile 1
4, 5, 6, 7
RD
DataPath 1
Mask 1
4, 5, 6, 7
Load Store Unit
WR
RegFile 0
0, 1, 2, 3
RD
DataPath 0
Mask 0
0, 1, 2, 3
503
505
502
506
504
Vector Mask
Register
501
500

FIG. 5

FIG. 6

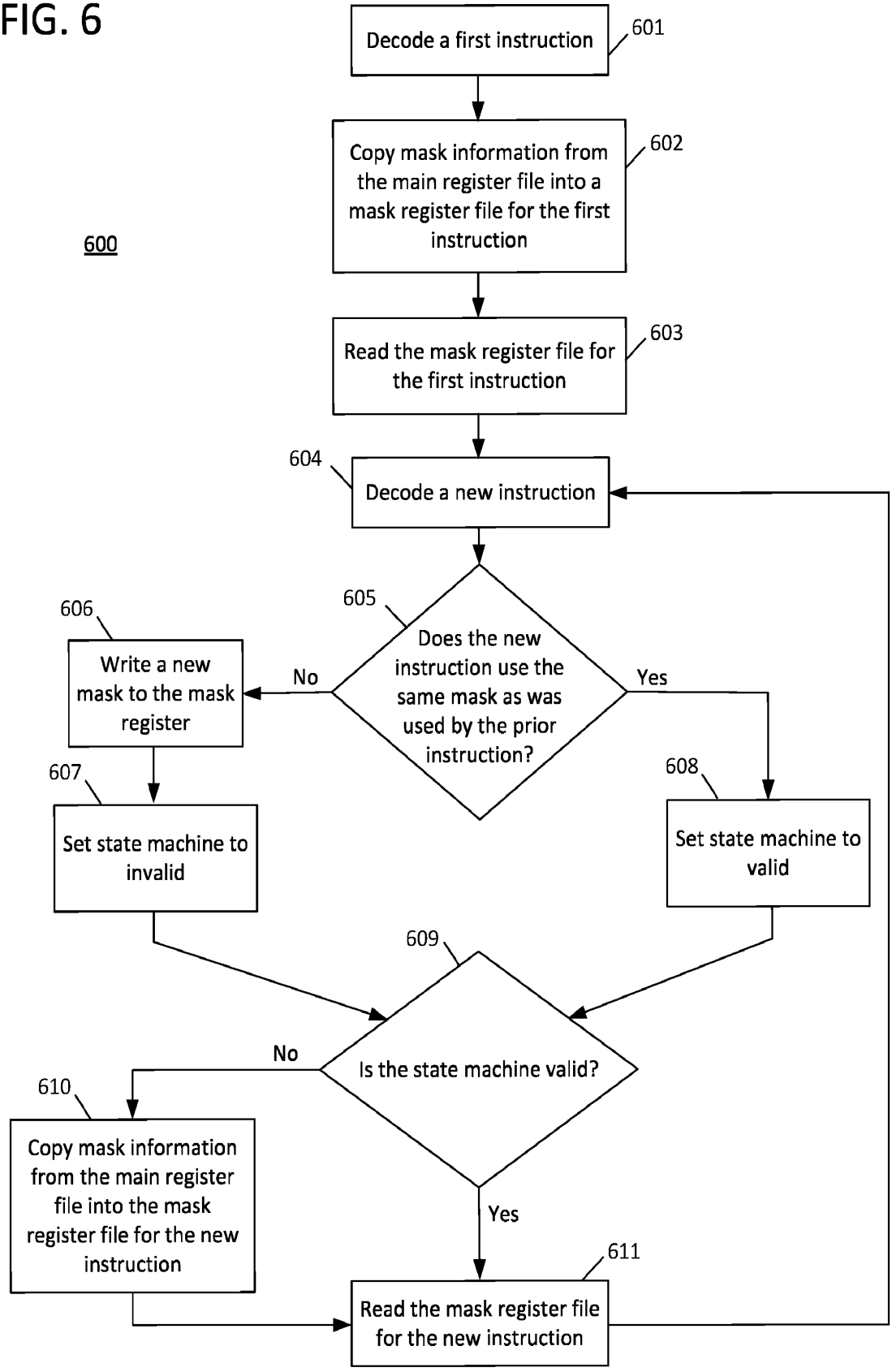

600
Decode a first instruction
601
Copy mask information from the main register file into a mask register file for the first instruction
602
Read the mask register file for the first instruction
603
604
Decode a new instruction
605
Does the new instruction use the same mask as was used by the prior instruction?
No
Yes
606
Write a new mask to the mask register
607
Set state machine to invalid
608
Set state machine to valid
609
Is the state machine valid?
No
Yes
610
Copy mask information from the main register file into the mask register file for the new instruction
611
Read the mask register file for the new instruction

FIG. 7

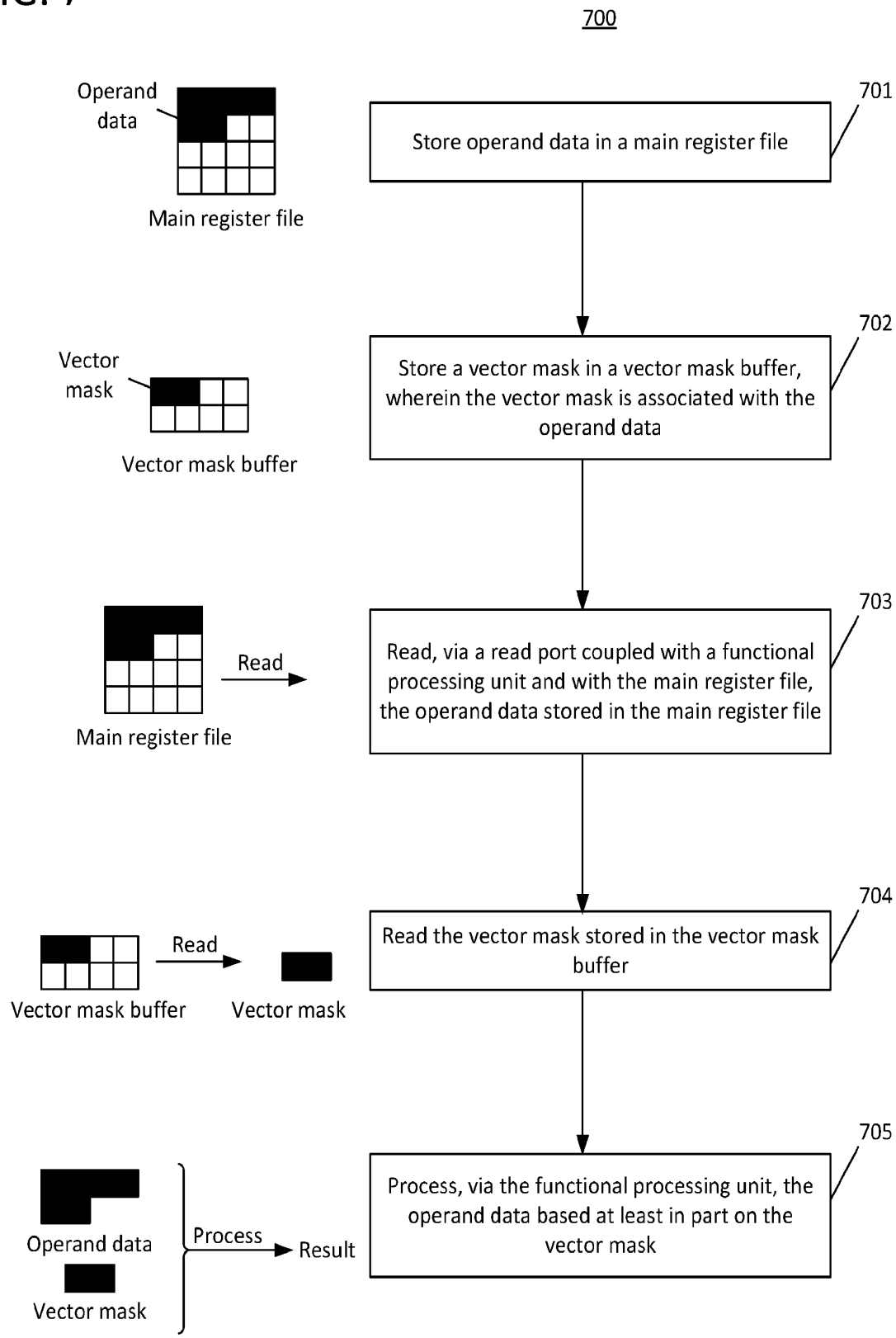

700
Operand data
Main register file
Store operand data in a main register file
701
Vector mask
Vector mask buffer
Store a vector mask in a vector mask buffer, wherein the vector mask is associated with the operand data
702
Main register file
Read
Read, via a read port coupled with a functional processing unit and with the main register file, the operand data stored in the main register file
703
Vector mask buffer
Read
Vector mask
Read the vector mask stored in the vector mask buffer
704
Operand data
Vector mask
Process
Result
Process, via the functional processing unit, the operand data based at least in part on the vector mask
705

FIG. 8

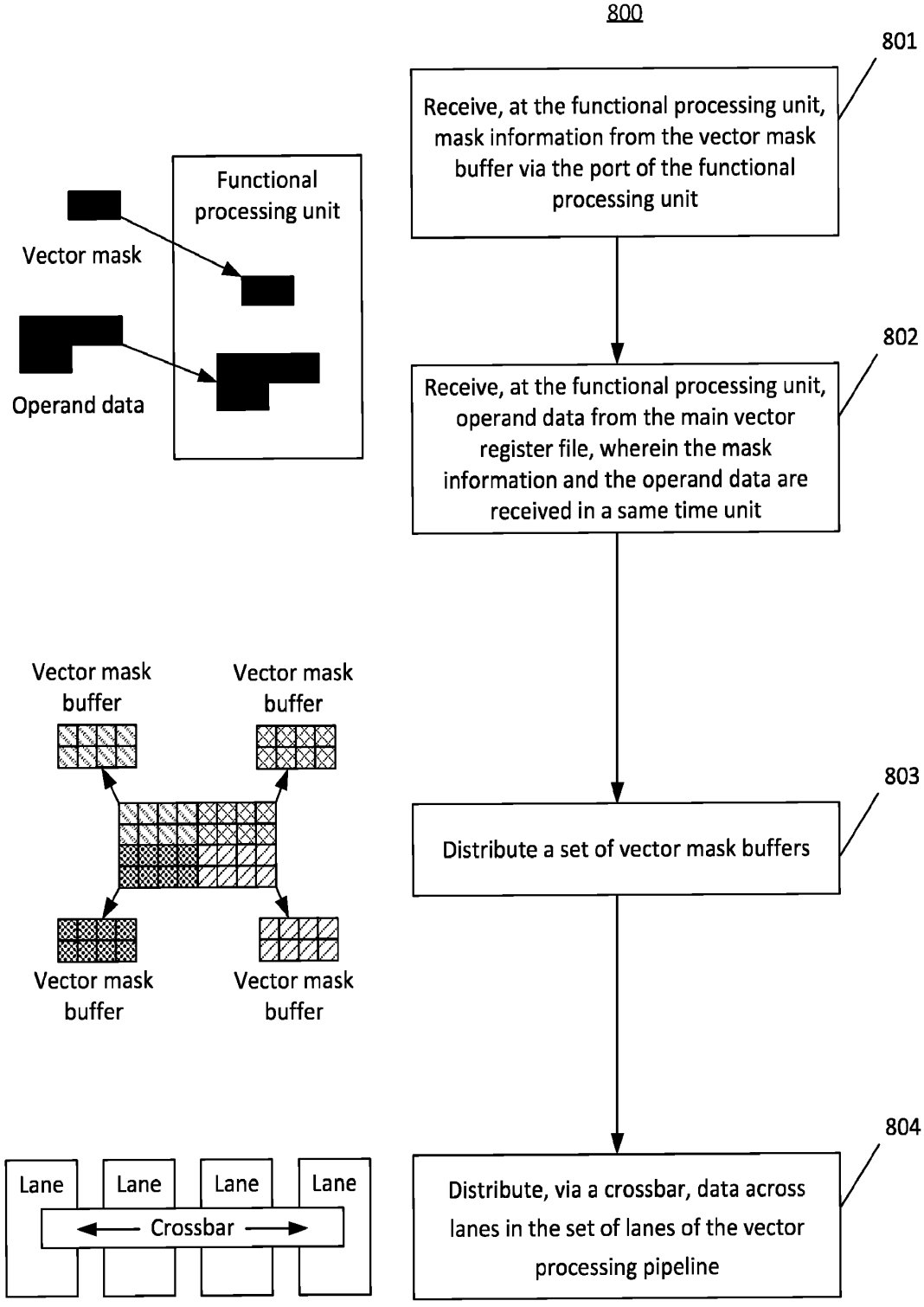
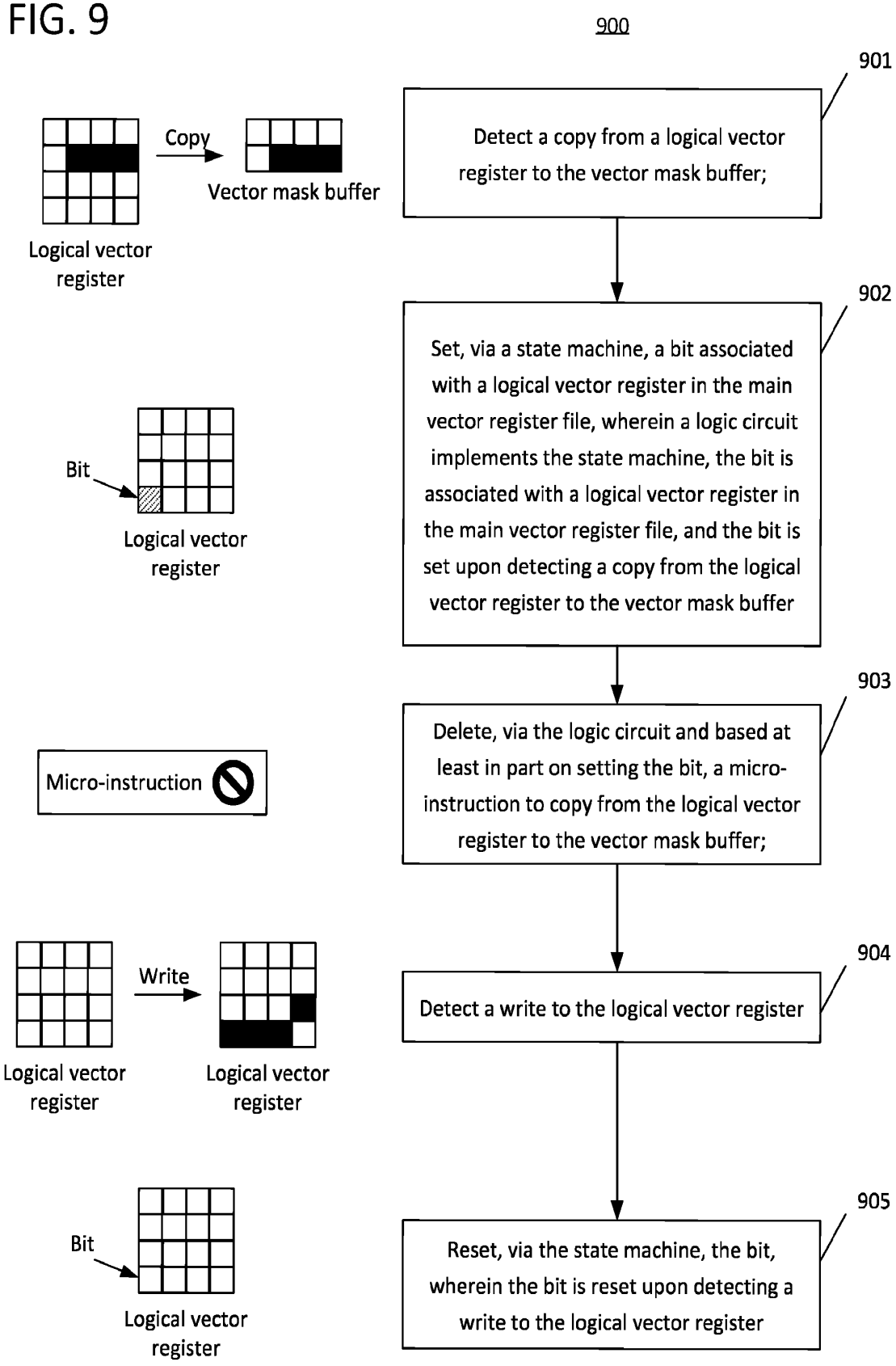

800
801
Receive, at the functional processing unit, mask information from the vector mask buffer via the port of the functional processing unit
802
Receive, at the functional processing unit, operand data from the main vector register file, wherein the mask information and the operand data are received in a same time unit
803
Distribute a set of vector mask buffers
804
Distribute, via a crossbar, data across lanes in the set of lanes of the vector processing pipeline
Functional processing unit
Vector mask
Operand data
Vector mask buffer
Vector mask buffer
Vector mask buffer
Vector mask buffer
Lane
Lane
Lane
Lane
Crossbar

FIG. 9


900
901
Detect a copy from a logical vector register to the vector mask buffer;
Copy
Vector mask buffer
Logical vector register
902
Set, via a state machine, a bit associated with a logical vector register in the main vector register file, wherein a logic circuit implements the state machine, the bit is associated with a logical vector register in the main vector register file, and the bit is set upon detecting a copy from the logical vector register to the vector mask buffer
Bit
Logical vector register
903
Delete, via the logic circuit and based at least in part on setting the bit, a micro-instruction to copy from the logical vector register to the vector mask buffer;
Micro-instruction
904
Detect a write to the logical vector register
Write
Logical vector register
Logical vector register
905
Reset, via the state machine, the bit, wherein the bit is reset upon detecting a write to the logical vector register
Bit
Logical vector register