CLAIMS

1. A polycrystalline silicon carbide support for a substrate intended to receive a power semiconductor device, the support comprising a first face, denoted “front face”, and a second face opposite the first and denoted “rear face”, the support comprising:
   - a first surface layer disposed directly under the front face and having resistivity that is greater than or equal to 1 ohm.cm; and
   - a second surface layer disposed directly under the rear face and having resistivity that is strictly less than 1 ohm.cm.

2. The polycrystalline silicon carbide support according to claim 1, wherein the second surface layer is 10 or more micrometres thick.

3. The polycrystalline silicon carbide support according to claim 1 or 2, wherein the second surface layer has a concentration of n-type dopants, such as nitrogen, that is greater than 10^20 at/cm^3.

4. The polycrystalline silicon carbide support according to claim 3, wherein the concentration of n-type dopants monotonically increases from the front face to the second surface layer.

5. The polycrystalline silicon carbide support according to any one of the preceding claims, wherein the first surface layer is not intentionally doped or has a

vanadium concentration that is greater than 10^15 at/cm^3.

6. The polycrystalline silicon carbide support according to any one of the preceding claims, having a total thickness, between the first face and the second face, ranging between 200 micrometres and 1 mm.

7. The polycrystalline silicon carbide support according to any one of the preceding claims, in the form of a circular wafer, advantageously with a diameter of 200 mm.

8. A substrate intended to receive a semiconductor device, comprising a support according to any one of the preceding claims and a seed layer transferred onto the front face of the support.

9. The substrate according to claim 8, wherein the seed layer is made up of gallium nitride, silicon carbide, sapphire or silicon.

10. The substrate according to claim 8 or 9, comprising a dielectric bonding layer disposed between, and in contact with, the support and the seed layer, preferably a dielectric bonding layer made of silicon nitride.

11. The substrate according to claim 8 or 9, wherein the seed layer is in direct contact with the support.

12. The substrate according to any one of claims 8 to 11, comprising a gallium nitride-based buffer layer, which preferably is semi-insulating, disposed on the seed layer.

13. The substrate according to claim 12, wherein the buffer layer is more than 3 microns thick, preferably more than 5 micrometres thick and even more preferably ranges between 5 micrometres and 10 micrometres thick.

14. The substrate according to claim 12 or 13, comprising a heterojunction disposed on the buffer layer, the heterojunction comprising a channel layer and a barrier layer and being capable of forming a 2D electron gas.

15. A semiconductor component, comprising a substrate according to claim 14, and a source structure, a drain structure, and a gate structure disposed on the heterojunction.

16. The semiconductor component according to the claim 15, comprising a metal sheet disposed under the rear face of the substrate, in ohmic contact with the second surface layer.

17. The semiconductor component according to claim 16, comprising an adhesion layer, such as a silver sintering paste layer, disposed between the metal sheet and the second surface layer.

18. The semiconductor component according to claim 16 or 17, comprising a metal layer disposed against the second surface layer.