

WHAT IS CLAIMED IS:

1. An electronic device comprising a semiconductor memory, wherein the semiconductor memory includes:

a first variable resistance layer including antimony (Sb);

a second variable resistance layer including antimony (Sb) with a content different from that of the first variable resistance layer; and

a first electrode interposed between the first variable resistance layer and the second variable resistance layer,

wherein the second variable resistance layer has a crystallization speed different from that of the first variable resistance layer according to a difference of contents of the antimony (Sb) included in the first and second variable resistance layers.

2. The electronic device of claim 1, wherein the second variable resistance layer has a crystallization speed higher than that of the first variable resistance layer.

3. The electronic device of claim 1, wherein the first variable resistance layer includes germanium (Ge) of 10 to 20 at%, antimony (Sb) of 20 to 25 at%, and tellurium (Te) of 45 to 55 at%, and

wherein the second variable resistance layer includes germanium (Ge) of 10 to 20 at%, antimony (Sb) of 25 to 30 at%, and tellurium (Te) of 45 to 55 at%.

4. The electronic device of claim 3, wherein the second variable resistance layer has a crystallization speed higher than that of the first variable resistance layer.

5. The electronic device of claim 1, wherein one or both of the first and second variable resistance layers include a doping element of 0 to 25

at%, and the doping element includes one or more of B, C, N, O, Si, Zn, Ga, As, Se, Ag, In, and Sn.

6. The electronic device of claim 1, wherein the second variable resistance layer is configured to selectively crystallize under an application of a first partial set pulse.

7. The electronic device of claim 6, wherein the first and second variable resistance layers are configured to crystallize under an application of a second partial set pulse for a period longer than that of the first partial set pulse.

8. The electronic device of claim 6, wherein the first partial set pulse and the second partial set pulse have different waveforms.

9. The electronic device of claim 1, further comprising:

a third variable resistance layer including antimony (Sb) with a content different from those of the first and second variable resistance layers; and

a second electrode interposed between the second variable resistance layer and the third variable resistance layer.

10. The electronic device of claim 9, wherein the first, second, and third variable resistance layers have different crystallization speeds.

11. The electronic device of claim 9, wherein the first variable resistance layer includes germanium (Ge) of 10 to 20 at%, antimony (Sb) of 20 to 25 at%, and tellurium (Te) of 45 to 55 at%,

wherein the second variable resistance layer includes germanium (Ge) of 10 to 20 at%, antimony (Sb) of 25 to 30 at%, and tellurium (Te) of

45 to 55 at%, and

wherein the third variable resistance layer includes germanium (Ge) of 10 to 20 at%, antimony (Sb) of 30 to 35 at%, and tellurium (Te) of 45 to 55 at%.

12. The electronic device of claim 11, wherein the first variable resistance layer further includes one or more of C, N, O, Si, Ga, As, and Se, and the third variable resistance layer further includes one or more of B, Zn, Ag, In, and Sn.

13. An electronic device comprising a semiconductor memory, wherein the semiconductor memory includes:

a first variable resistance layer including antimony (Sb);

a second variable resistance layer including antimony (Sb) with a content higher than that of the first variable resistance layer;

a third variable resistance layer including antimony (Sb) with a content higher than that of the second variable resistance layer;

a first electrode interposed between the first variable resistance layer and the second variable resistance layer; and

a second electrode interposed between the second variable resistance layer and the third variable resistance layer,

wherein the second variable resistance layer has a crystallization speed higher than that of the first variable resistance layer according to a difference of contents of the antimony (Sb) included in the first and second variable resistance layers, and

wherein the third variable resistance layer has a crystallization speed higher than that of the second variable resistance layer according to a difference of contents of the antimony (Sb) included in the second and third variable resistance layers.

14. The electronic device of claim 13, wherein one or more of the first, second, and third variable resistance layers further include a doping element of 0 to 25 at%.

15. The electronic device of claim 14, wherein the doping element includes one or more of B, C, N, O, Si, Zn, Ga, As, Se, Ag, In, and Sn.

16. The electronic device of claim 13, wherein the first variable resistance layer further includes one or more of C, N, O, Si, Ga, As, and Se, and the third variable resistance layer further includes one or more of B, Zn, Ag, In, and Sn.

17. The electronic device of claim 13, wherein the third variable resistance layer is configured to selectively crystallize under an application of a first partial set pulse, the second and third variable resistance layers are configured to selectively crystallize under an application of a second partial set pulse for a period longer than that of the first partial set pulse, and the first, second, and third variable resistance layers are configured to crystallize under an application of a fully set pulse for a period longer than each of those of the first partial set pulse and the second partial set pulse.

18. The electronic device of claim 13, wherein the first, second, and third variable resistance layers are configured to reset under an application of a reset pulse.

19. An electronic device comprising a semiconductor memory, wherein the semiconductor memory includes:

- a first variable resistance layer;

- a second variable resistance layer having a crystallization speed different from that of the first variable resistance layer; and

a first electrode interposed between the first variable resistance layer and the second variable resistance layer,

wherein the second variable resistance layer includes antimony (Sb) with a content higher than a content of the antimony (Sb) included in the first variable resistance layer,

wherein the second variable resistance layer has a crystallization speed different from that of the first variable resistance layer according to a difference of contents of the antimony (Sb) included in the first and second variable resistance layers, and

wherein the first variable resistance layer, or the second variable resistance layer, or both further include a first doping element which decreases a crystallization speed of a variable resistance material or a second doping element which increases the crystallization speed.

20. The electronic device of claim 19, wherein the first variable resistance layer includes the first doping element, and the second variable resistance layer has a crystallization speed higher than that of the first variable resistance layer.

21. The electronic device of claim 20, wherein the first doping element of the first variable resistance layer includes one or more of C, N, O, Si, Ga, As, and Se.

22. The electronic device of claim 19, wherein the second variable resistance layer includes the second doping element, and has a crystallization speed higher than that of the first variable resistance layer.

23. The electronic device of claim 22, wherein the second doping element of the second variable resistance layer includes one or more of B, Zn, Ag, In, and Sn.

24. A method for operating an electronic device including a semiconductor memory, wherein the semiconductor memory includes a first variable resistance layer including antimony (Sb), a second variable resistance layer including antimony (Sb) with a content higher than that of the first variable resistance layer, and a first electrode interposed between the first variable resistance layer and the second variable resistance layer, the method comprising:

selectively crystallizing the second variable resistance layer by applying a first partial set pulse,

wherein the second variable resistance layer has a crystallization speed higher than that of the first variable resistance layer according to a difference of contents of the antimony (Sb) included in the first and second variable resistance layers.

25. The method of claim 24, wherein the semiconductor memory further includes a third variable resistance layer including antimony (Sb) with a content higher than each of those of the first and second variable resistance layers and a second electrode interposed between the second variable resistance layer and the third variable resistance layer, the method further comprising:

selectively crystallizing the second variable resistance layer and the third variable resistance layer by applying a second partial set pulse for a period longer than that of the first partial set pulse; and

crystallizing the first, second, and third variable resistance layers by applying a fully set pulse for a period longer than each of those of the first partial set pulse and the second partial set pulse.

26. The method of claim 25, further comprising resetting the first variable resistance layer, the second variable resistance layer, and the third variable resistance layer by applying a reset pulse.