CLAIMS

What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A method of forming an integrated structure, the method comprising the acts of:

forming an isolation region in a first substrate;

forming a photonics area on a second substrate; and

bonding the first and second substrates together such that the isolation region is aligned with the photonics area.

2. A method as in claim 1, wherein the first and second substrates each comprise a silicon substrate, the photonics area being a silicon photonics area.

3. A method of claim 2, further comprising forming a waveguide within the silicon photonics area such that the waveguide core is aligned with the isolation region.

4. A method as in claim 3, wherein the waveguide is formed after the first and second substrates are bonded together.

5. A method as in claim 2, further comprising forming the isolation region as a shallow trench isolation region.

6. A method as in claim 5, further comprising forming a BOX as part of said second substrate beneath the silicon photonics area, wherein the combined thickness of the BOX and shallow trench isolation region is at least 1 um.

7. A method as in claim 6, wherein the thickness of the BOX is less than or equal to 200 nm.

8. A method as in claim 6, wherein the thickness of the shallow trench isolation region is in the range of about 800 nm to about 1200 nm.

9. A method as in claim 3, further comprising forming a cladding region to surround the waveguide core, the cladding region being formed at least in part by a first dielectric on the second substrate located below the waveguide.

10. A method as in claim 9, wherein the waveguide core is formed of silicon and the first dielectric comprises an oxide.

11. A method as in claim 10, wherein the first dielectric comprises silicon dioxide.

12. A method as in claim 9, wherein the cladding region further comprises a second dielectric on the sides of the waveguide.

13. A method as in claim 10, wherein said first and second dielectrics comprise silicon dioxide.

14. A method as in claim 2, wherein the bonding further comprises forming an amorphous silicon on at least one of the first and second substrates and pressing the substrates together such that the amorphous silicon functions as a bonding material to bond the first substrate to the second substrate.

15. A method as in claim 2,wherein the second substrate further comprises an insulator, and the bonding of the first and second substrates forms a silicon-on-insulator structure having a buried insulator.

16. A method as in claim 2, wherein the second substrate further comprises dielectric material adjacent the silicon, the method further comprising thinning the second substrate silicon before the waveguide is formed.

17. A method as in claim 16, wherein the second substrate silicon is thinned by implanting a dopant to form a cleave line and then cleaving along the cleave line to remove a portion of the silicon.

18. A method as in claim 17, further comprising recycling the removed portion of the second substrate silicon for use as a substrate in another integrated structure.

19. A method as in claim 2, comprising thinning the first substrate from a side opposite a side containing the trench isolation region.

20. A method as in claim 19, wherein the thinning of the first substrate comprises implanting a dopant into the silicon of the first substrate to form a cleave line and then cleaving the silicon of the first substrate along the cleave line to remove a portion of the silicon.

21. A method as in claim 20, further comprising recycling the removed portion of the silicon of the first substrate for use as a substrate in another integrated structure.

22. A method as in claim 1, wherein the first and second substrates comprise a semiconductor material with the photonics area being formed of the semiconductor material of the second substrate, said method further comprising forming a waveguide core using the semiconductor material of the second substrate.

23. A method as in claim 22, wherein the semiconductor material comprises silicon.

24. A method as in claim 1, further comprising forming a circuit element area on the second substrate.

25. An integrated structure comprising:

a first semiconductor substrate having a shallow trench isolation region formed therein, the trench of the isolation region being filled with a dielectric material having a first index of refraction; and

a second substrate attached to the first substrate and including a dielectric material facing the first substrate and a waveguide formed of a semiconductor material over the dielectric material, the waveguide being formed of a material having a second index of refraction greater than the first index of refraction and being located over the shallow trench isolation region.

26. A structure as in claim 25, wherein the shallow trench isolation region comprises silicon dioxide within the trench.

27. A structure as in claim 25, wherein the combined thickness of the dielectric material facing the second substrate and the shallow trench isolation region is at least 1000 nm.

28. A structure as in claim 25, wherein the first and second substrates comprise silicon.

29. A structure as in claim 25, wherein the waveguide comprises a core region surrounded by a cladding region, the cladding region being formed at least in part by the dielectric material on the second substrate.

30. A structure as in claim 25, wherein the core region comprises silicon and the cladding region comprises silicon dioxide.

31. A structure as in claim 25, further comprising an area of the semiconductor material of the second substrate on which an electronic circuit element is formed.

32. A structure as in claim 25, wherein the attached first and second substrates form a silicon-on-insulator structure.

33. A structure as in claim 23, further comprising a dielectric material over the semiconductor material of the second substrate.

34. A structure as in claim 33, wherein the dielectric material over the semiconductor material of the second substrate is part of an interlayer dielectric structure.

CLAIMS

1. A method of forming an integrated structure, the method comprising the acts of:

forming a shallow trench isolation region in an upper surface of a first substrate;

forming a photonics area on a second substrate; and

bonding the first and second substrates together such that the upper surface of the first substrate faces the second substrate and the shallow trench isolation region is aligned with the photonics area.

2. A method as in claim 1, wherein the first and second substrates each comprise a silicon substrate, the photonics area being a silicon photonics area.

3. A method of claim 2, further comprising forming a waveguide within the silicon photonics area of the bonded substrates, the waveguide including a waveguide core and cladding, with the waveguide core being aligned with the shallow trench isolation region of the bonded substrates.

4. A method as in claim 3, wherein the waveguide is formed after the first and second substrates are bonded together.

5. A method as in claim 3, further comprising, prior to said bonding: forming a BOX as part of said second substrate, which is beneath the waveguide core of the bonded substrates, wherein the combined thickness of the BOX and shallow trench isolation region is at least 1 um, the bonded substrates forming a silicon-on-insulator structure.

6. A method as in claim 5, wherein the thickness of the BOX is less than or equal to 200 nm.

7. A method as in claim 5, wherein the thickness of the shallow trench isolation region is in the range of about 800 nm to about 1200 nm.

8. A method as in claim 3, further comprising forming a cladding region to surround the waveguide core, the cladding region being formed at least in part by a first dielectric on the second substrate located below the waveguide.

9. A method as in claim 8, wherein the waveguide core is formed of silicon and the first dielectric comprises an oxide.

10. A method as in claim 9, wherein the first dielectric comprises silicon dioxide.

11. A method as in claim 8, wherein the cladding region further comprises a second dielectric on the sides of the waveguide.

12. A method as in claim 9, wherein said first and second dielectrics comprise silicon dioxide.

13. A method as in claim 2, wherein the bonding further comprises forming an amorphous silicon on at least one of the first and second substrates and pressing the substrates together such that the amorphous silicon functions as a bonding material to bond the first substrate to the second substrate.

14. A method as in claim 2, wherein the second substrate further comprises an insulator, and the bonding of the first and second substrates forms a silicon-on-insulator structure having a buried insulator.

15. A method as in claim 2, wherein the second substrate further comprises dielectric material adjacent the silicon, the method further comprising thinning the second substrate silicon before the waveguide is formed.

16. A method as in claim 15, wherein the second substrate silicon is thinned by implanting a dopant to form a cleave line and then cleaving along the cleave line to remove a portion of the silicon.

17. A method as in claim 16, further comprising recycling the removed portion of the second substrate silicon for use as a substrate in another integrated structure.

18. A method as in claim 2, comprising thinning the first substrate from a side opposite a side containing the shallow trench isolation region.

19. A method as in claim 18, wherein the thinning of the first substrate comprises implanting a dopant into the silicon of the first substrate to form a cleave line and then cleaving the silicon of the first substrate along the cleave line to remove a portion of the silicon.

20. A method as in claim 19, further comprising recycling the removed portion of the silicon of the first substrate for use as a substrate in another integrated structure.

21. A method as in claim 1, wherein the first and second substrates comprise a semiconductor material with the photonics area being formed of the semiconductor material of the second substrate, said method further comprising forming a waveguide core using the semiconductor material of the second substrate.

22. A method as in claim 21, wherein the semiconductor material comprises silicon.

23. A method as in claim 1, further comprising forming a circuit element area on the second substrate.

24. An integrated structure comprising:

a first semiconductor substrate having a shallow trench isolation region formed therein, the trench of the isolation region being filled with a dielectric material having a first index of refraction; and

a second substrate attached to the first substrate and including a dielectric material facing the first substrate and a waveguide having a core formed of a semiconductor material over the dielectric material, the waveguide core being formed of a material having a second index of refraction greater than the first index of refraction and being located over the shallow trench isolation region.

25. A structure as in claim 24, wherein the shallow trench isolation region comprises silicon dioxide within the trench.

26. A structure as in claim 24, wherein the combined thickness of the dielectric material facing the second substrate and the shallow trench isolation region is at least 1000 nm.

27. A structure as in claim 24, wherein the first and second substrates comprise silicon.

28. A structure as in claim 24, wherein the waveguide comprises the core surrounded by a cladding region, the cladding region being formed at least in part by the dielectric material on the second substrate.

29. A structure as in claim 24, wherein the core comprises silicon and the cladding region comprises silicon dioxide.

30. A structure as in claim 24, further comprising an area of the semiconductor material of the second substrate on which an electronic circuit element is formed.

31. A structure as in claim 24, wherein the attached first and second substrates form a silicon-on-insulator structure.

32. A structure as in claim 22, further comprising a dielectric material over the semiconductor material of the second substrate.

33. A structure as in claim 32, wherein the dielectric material over the semiconductor material of the second substrate is part of an interlayer dielectric structure.