We claim:

**1**. A method of forming a NAND unit cell, comprising:

forming vertical columns of a semiconductor material over a substrate, the columns comprising alternating n-type doped layers of the semiconductor material and p-type doped layers of the semiconductor material; each of the columns comprising at least four layers of the n-type doped semiconductor material and at least three layers of the p-type doped semiconductor material; each of the columns extending vertically away from the substrate with a first one of the doped layers being nearer to the substrate than the other doped layers and the other doped layers being above both the substrate and the first one of the doped layers;

after forming the columns that comprise at least four layers of the n-type doped semiconductor material in alternating relationship with at least three layers of the p-type doped semiconductor material, lining the columns with, in sequential order, a layer of tunnel dielectric, a layer of charge-storage material, and a layer of charge-blocking material, the layer of tunnel dielectric forming an upward-opening container; and

forming alternating layers of electrically insulative material and electrically conductive material between the lined columns and within the opening within the container; the layers of electrically conductive material forming a plurality of horizontally-spaced control gate structures within the opening within the container; at least some of the control gate structures being incorporated into string devices of the NAND unit cell, wherein a first control gate structure of the plurality of control gate structures within the container is spaced from a second control gate structure of the plurality of control gate structures within the container that is immediately adjacent the first control gate structure only by the electrically insulative material and wherein the forming of the alternating layers of electrically insulative material and electrically conductive material comprises forming the first control gate structure above the layer of charge-blocking material and forming the second control gate structure above the first control gate structure.

**2**. The method of claim **1** wherein some of the control gate structures are incorporated into selecting devices of the NAND unit cell.

**3**. The method of claim **1** wherein all of the control gate structures are incorporated into string devices, and further comprising forming selecting devices which are above and below the string devices, the selecting devices comprising control gates that are spaced from the lined columns only by the tunnel dielectric.

**4**. The method of claim **1** wherein the substrate comprises monocrystalline silicon, and wherein the forming the vertical columns comprises:

epitaxially growing alternating layers of n-type doped semiconductor material and p-type doped semiconductor material over the substrate, with a first of the alternating layers being grown on the monocrystalline silicon of the substrate; and

patterning the epitaxially-grown layers into the vertical columns.

**5**. The method of claim **4** wherein the patterning the vertical columns comprises:

forming at least one first trench in the epitaxially-grown layers, with the at least one first trench extending along a first horizontal direction;

filling the at least one first trench with electrical isolation material;

after filling the at least one first trench, forming second trenches that extend into the epitaxially-grown layers and the electrical isolation material, with the second trenches extending along a second horizontal direction that is orthogonal to the first horizontal direction;

wherein the lining the columns comprises forming the layers of tunnel dielectric, charge-storage material, and blocking dielectric within the second trenches; and

wherein the alternating layers of electrically insulative material and electrically conductive material are formed within the second trenches.

**6**. The method of claim **1** wherein the n-type layers have substantially the same thickness as the p-type layers.

**7**. The method of claim **1** wherein at least one of the p-type layers is incorporated into a selecting device of the NAND unit cell and at least one of the p-type layers is incorporated into a string device of the NAND unit cell and wherein a sidewall of the one p-type layer is collinear with a line that is collinear with a sidewall of the one n-type layer.

**8**. A method of forming a NAND unit cell, comprising:

forming a layer of tunnel dielectric material between a pair of vertical structures; the tunnel dielectric material layer forming an upward-opening container; the vertical structures comprising alternating layers of n-type doped semiconductor material and p-type doped semiconductor material;

forming a layer of charge-storage material within the container;

forming a layer of charge-blocking material within the container and over the layer of charge-storage material; the layers of charge-storage material and charge-blocking material narrowing the container and leaving an opening within the container; and

forming alternating layers of electrically insulative material and electrically conductive material within the opening within the container; the layers of electrically conductive material forming a plurality of spaced apart control gate structures within the opening within the container which are incorporated into selecting devices of the NAND unit cell, wherein a first control gate structure of the plurality of control gate structures within the container is spaced from a second control gate structure of the plurality of control gate structures within the container that is immediately adjacent the first control gate structure only by the electrically insulative material and wherein the forming of the alternating layers of electrically insulative material and electrically conductive material comprises forming the first control gate structure above the layer of charge-blocking material and forming the second control gate structure above the first control gate structure.

**9**. The method of claim **8** wherein the forming the layer of tunnel dielectric material comprises:

deposition of the tunnel dielectric material over the pair of vertical structures and within a trench between the vertical structures; and

planarization of the tunnel dielectric material to remove the tunnel dielectric material from over the pair of vertical structures.

**10**. The method of claim **8** wherein the forming the layer of tunnel dielectric material, charge-storage material, and charge-blocking material comprises:

deposition of the tunnel dielectric material over the pair of vertical structures and within a trench between the vertical structures;

deposition of the charge-storage material over the pair of vertical structures and within a trench between the vertical structures;

deposition of the charge-blocking material over the pair of vertical structures and within a trench between the vertical structures; and

planarization of the tunnel dielectric material, charge-storage material, and charge-blocking material to remove the tunnel dielectric material, charge-storage material, and charge-blocking material from over the pair of vertical structures.

**11**. The method of claim **8** wherein the spaced apart control gate structures are formed to horizontally align with only the p-type doped semiconductor material so that the control gate structures do not overlap the layers of n-type doped semiconductor material.

**12**. The method of claim **8** wherein:

the layers of electrically conductive material are formed to extend laterally beyond the NAND unit cell;

a plurality of interconnects are formed to be in one-to-one correspondence with the layers of electrically conductive material;

the layers of conductive material form a series of steps at one lateral end, with steps progressively becoming more laterally inward in going from lower layers of conductive material to upper layers of conductive material to leave exposed platforms at said one lateral end of the layers of conductive material; and

the interconnects are formed to electrically contact the conductive layers at the exposed platforms.