NEGATIVE COEFFICIENT THERMAL EXPANSION MATERIALS FOR DYNAMIC BOW COMPENSATION APPLICATION

INCORPORATION BY REFERENCE

[0001] A PCT Request Form is filed concurrently with this specification as part of the present application. Each application that the present application claims benefit of or priority to as identified in the concurrently filed PCT Request Form is incorporated by reference herein in their entireties and for all purposes.

BACKGROUND

[0002] In semiconductor processing, it may be desired that a wafer remains substantially flat. However, during normal operations, a wafer may experience wafer bow. The wafer bow may cause issues such as improper clamping by an electrostatic chuck, inability to be held by a wafer handler, pattern transfer issues during photolithography issues, and others. Processes have been developed to manage wafer bow by keeping the wafer flat within process tolerances. One process includes depositing a film on the backside of the wafer to counteract any stress that may be causing the wafer to bow.

[0003] The background description provided herein is for the purposes of generally presenting the context of the disclosure. Work of the presently named inventors, to the extent it is described in this background section, as well as aspects of the description that may not otherwise qualify as prior art at the time of filing, are neither expressly nor implicitly admitted as prior art against the present disclosure.

SUMMARY

[0004] Disclosed herein are methods and systems of depositing films. In one aspect of the embodiments herein, a method of reducing bow in a substrate is provided, the method including: receiving a substrate having one or more frontside layers on a frontside of the substrate, wherein the substrate has a bow; depositing one or more backside layers, wherein the one or more backside layers include a material having a negative thermal expansion coefficient.

[0005] In some embodiments, the one or more backside layers include mixed metal oxides of Scandium, Tungsten, Zirconium, or any combinations thereof. In some embodiments, the one or more backside layers compensate for a dynamic wafer bow of the substrate as the substrate is heated. In some embodiments, the internal tensile stress of the one or more backside layers increase when the one or more backside layers are heated. In some embodiments, the one or more frontside layers would cause a change in bow when the substrate is heated to temperatures above about 400°C, and wherein the one or more backside layers compensate the change in bow from the one

or more frontside layers when heated to temperatures above about 400°C. In some embodiments, the one or more frontside layers have a first thermal stress shift, the one or more backside layers have a second thermal stress shift, and wherein the second thermal stress shift is more than the first thermal stress shift. In some embodiments, the one or more backside layers have a tensile internal stress at ambient temperatures. In some embodiments, the one or more backside layers have a neutral internal stress at ambient temperatures. In some embodiments, the method further includes depositing an additional backside layer, wherein the additional backside layer compensates bow at ambient temperature. In some embodiments, the bow of the substrate caused by the one or more frontside layers is about 300μm or more. In some embodiments, at least one of the one or more frontside layers includes a hardmask. In some embodiments, the one or more frontside layers include a stack of about 100 or more alternating layers. In some embodiments, the stack includes alternating oxide layers and nitride or polysilicon layers. In some embodiments, the backside layer has a thickness of about 0.1 μm to about 5 μm.

[0006] In another aspect of the embodiments herein, a substrate is provided, including: one or more frontside layers on a frontside of the substrate; one or more backside layers, wherein the one or more backside layers have a negative thermal expansion coefficient. In some embodiments, the one or more backside layers include mixed metal oxides of Scandium, Tungsten, Zirconium, or any combinations thereof. In some embodiments, the one or more backside layers compensate for dynamic wafer bow of the substrate as the substrate is heated. In some embodiments, the one or more frontside layers have a first thermal stress shift, the one or more backside layers have a second thermal stress shift, and wherein the second thermal stress shift is more than the first thermal stress shift. In some embodiments,, if internal stress from the one or more frontside layers are not compensated by the one or more backside layers at temperatures greater than about 500°C, the substrate has a bow of about 300 μm or more. In some embodiments, the one or more backside layers have a thickness of about 0.1 μm to about 3 μm. In some embodiments, including an additional backside layer, wherein the additional backside layer compensates a wafer bow caused by the one or more frontside layers, and wherein the backside layer does not compensate the wafer bow at ambient temperatures.

[0007] In another aspect of the embodiments herein, an apparatus for semiconductor processing is provided, the apparatus including: a process chamber; and a controller including memory and processors configured for: receiving a substrate having one or more frontside layers on a frontside of the substrate, wherein the substrate has a bow; depositing one or more backside layers, wherein the one or more backside layers have a negative thermal expansion coefficient.

[0008] These and other features of the disclosed embodiments will be described in detail below

with reference to the associated drawings.

BRIEF DESCRIPTION OF DRAWINGS

[0009] Figures 1A and 1B show examples of unbowed and bowed semiconductor wafers on an electrostatic chuck.

[0010] Figures 2A-B are flowcharts illustrating example operations for reducing substrate bow for various embodiments herein.

[0011] Figures 3A-B are diagrams illustrating backside bow from films deposited according to various embodiments herein.

[0012] Figures 4A-C are diagrams illustrating dynamic bow compensation according to various embodiments herein.

[0013] Figure 5 is a chart illustrating an estimate of wafer bowing for an oxide/nitride layers, a negative thermal expansion coefficient layer, and a combined layer according to various embodiments herein.

[0014] Figures 6A and 6B show a block diagram of an example substrate processing system.

[0015] Figure 7A shows an example cross section of an edge of a shower-pedestal.

[0016] Figure 7B shows a top view of an example carrier ring.

[0017] Figure 8 shows a schematic of an example process system that may be used to perform the methods described herein.

DETAILED DESCRIPTION

Terminology

[0018] The following terms are used throughout the instant specification:

[0019] The terms "semiconductor wafer," "wafer," "substrate," "wafer substrate" and "partially fabricated integrated circuit" may be used interchangeably. Those of ordinary skill in the art understand that the term "partially fabricated integrated circuit" can refer to a semiconductor wafer during any of many stages of integrated circuit fabrication thereon. A wafer or substrate used in the semiconductor device industry typically has a diameter of 200 mm, 300 mm, or 450 mm. Examples of wafer materials include silicon (Si), gallium arsenide (GaAs), and silicon germanium (SiGe). Besides semiconductor wafers, other workpieces that may take advantage of the disclosed embodiments include various articles such as printed circuit boards, magnetic recording media, magnetic recording sensors, mirrors, optical elements, display devices or components such as backplanes for pixelated display devices, flat panel displays, micro-mechanical devices and the

like. The workpiece may be of various shapes, sizes, and materials.

[0020] The flow rates and power levels provided herein are appropriate for processing on 300 mm substrate, unless otherwise specified. It should be noted that these flows and power levels may be adjusted as necessary for substrates of other sizes. The following detailed description assumes that certain implementations may occur on a wafer. However, the implementations are not so limited. The work piece may be of various shapes, sizes, and materials. In addition to semiconductor wafers, other work pieces that may take advantage of at least certain various implementations include various articles such as printed circuit boards and the like.

[0021] A "semiconductor device fabrication operation" as used herein is an operation performed during fabrication of semiconductor devices. Typically, the overall fabrication process includes multiple semiconductor device fabrication operations, each performed in its own semiconductor fabrication tool such as a plasma reactor, an electroplating cell, a chemical mechanical planarization tool, a wet etch tool, and the like. Categories of semiconductor device fabrication operations include subtractive processes, such as etch processes and planarization processes, and material additive processes, such as deposition processes (e.g., physical vapor deposition, chemical vapor deposition, atomic layer deposition, electrochemical deposition, electroless deposition). In the context of etch processes, a substrate etch process includes processes that etch a mask layer or, more generally, processes that etch any layer of material previously deposited on and/or otherwise residing on a substrate surface. Such an etch process may etch a stack of layers in the substrate.

[0022] "Manufacturing equipment" refers to equipment in which a manufacturing process takes place. Manufacturing equipment often has a process chamber in which the workpiece resides during processing. Typically, when in use, manufacturing equipment performs one or more semiconductor device fabrication operations. Examples of manufacturing equipment for semiconductor device fabrication include deposition reactors such as electroplating cells, physical vapor deposition reactors, chemical vapor deposition reactors, and atomic layer deposition reactors, and subtractive process reactors such as dry etch reactors (e.g., chemical and/or physical etch reactors), wet etch reactors, and ashers.

[0023] "Wafer bow" as used herein may refer to a deformation of a wafer. The deformation may have radial and/or azimuthal components. Examples of types of wafer bow include dome shapes, bowl shapes, and saddle shapes. Wafer bow may occur during fabrication, for example, as a result of stress to the wafer during deposition of materials on an active surface of a wafer substrate. Wafer bow may occur during various types of fabrication, such as when large stacks of

materials are deposited. Wafer bow may cause complications in subsequent processing steps. For example, the wafer may fail to chuck correctly if an amount of bowing is too large. Moreover, some processing steps (e.g., photolithography) may produce poor results if performed on a wafer that is excessively bowed.

[0024] Wafer bow may be measured as a deviation of the mean or median distance of the surface of the wafer to a reference plane. In some embodiments, the point of the median surface of the wafer may be the center point (e.g., in the case of concave or domed bowing), or an edge point of the wafer and/or an average edge point of the wafer (e.g., in the case of warping or convex bowing). In some embodiments wafer bow may be measured from a reference plane such that when an edge point of the wafer is below the reference plane the edge point is considered to have a negative bow, and when the edge point of the wafer is above the reference plane the edge point is considered to have a positive bow. In some embodiments, positive or negative bow may be measured along a z axis perpendicular to the reference plane.

[0025] "Thermal stress shift" as used herein may refer to a change in the internal stress of one or more layers deposited on a wafer as a result of changes in temperature of the wafer. A wafer and one or more layers deposited on the wafer generally have different thermal expansion coefficients (CTE). As the wafer is heated, the difference in expansion between the wafer and the one or more layers may change the internal stress of the one or more layers and thus change the bowing of the wafer. This may be problematic as a wafer that is substantially flat at ambient temperature may then bow at elevated temperatures. A thermal stress shift may be an increase (tensile) or decrease (compressive) in internal stress.

[0026] "Dynamic wafer bow" as used herein refers to a change in wafer bow from changing process conditions, e.g., temperature. As temperature increases from ambient temperature to processing temperatures, a thermal stress shift occurs that changes wafer bow caused by frontside and/or backside layers. In some embodiments, a thermal stress shift may correspond with a dynamic wafer bow between two temperatures. For example, a 450 μm dynamic wafer bow may refer to a change in wafer bow of 450 μm when the wafer is heated from ambient temperature to a processing temperature, e.g., 650 °C. Dynamic wafer bow may be also result in wafer bow that causes the wafer bow to change from an umbrella shape to a bowl shape, i.e., the sign of the wafer bow may change from negative to positive, as the bow may change from -200μm to +250μm for a 450μm dynamic wafer bow. The relationship between dynamic wafer bow and thermal stress shifts may generally be linear. While a thermal stress shift is related to the internal stress of a film, dynamic wafer bow is additionally dependent on the thickness of the film. Two films of different thicknesses may experience the same thermal stress shift upon heating, but the dynamic wafer bow

caused by each film will differ because of the different thicknesses. Thus, a film having a higher thermal stress shift may be thin while having the same dynamic wafer bow as a thicker film with a lower thermal stress shift.

Bowed Wafers

[0027] Semiconductor device fabrication often involves deposition of a stack of layers on a wafer substrate. Typically, most deposition and other processing to form the devices occurs on one side of the substrate, often referred to as the front face or frontside of a wafer. As the deposited layers build up, they can introduce stress in the wafer. A large net tensile or compressive stress can cause the wafer to bow, which is undesirable.

[0028] Bowing is especially likely to occur where large stacks of materials are deposited, for example, in the context of 3D-NAND devices, or where a thick front side layer is deposited. Where bowing is significant, it can deleteriously affect subsequent processing steps. For instance, the wafer may fail to chuck correctly if the bowing is too great. Figures 1A and 1B show a wafer on an electrostatic chuck. Figure 1A shows a wafer 102 on an electrostatic chuck 110. When the wafer 102 is substantially flat for purposes of a particular process operation, e.g., having a bow of about 100 μm or less, the wafer may be properly clamped, securing the wafer for subsequent processing steps. Figure 1B shows a bowed wafer 104 on the electrostatic chuck 110. When the bow is significant, the wafer may fail to secure properly on the electrostatic chuck. Wafer bow may cause other problems. For example, certain processing steps (e.g., photolithography) are very precise and produce poor results if the wafer is not substantially flat. The problem may be manifest as lithography defocus.

[0029] One example stack that may cause these problems is a stack having alternating layers of oxide and nitride (e.g., silicon oxide/silicon nitride/silicon oxide/silicon nitride, etc.). Another example of a type of stack likely to cause bowing includes alternating layers of oxide and polysilicon (e.g., silicon oxide/polysilicon/silicon oxide/polysilicon, etc.). Other examples of stack materials that may be problematic include, but are not limited to, tungsten and titanium nitride.

[0030] The materials in the stacks may be deposited through chemical vapor deposition (CVD) techniques such as plasma enhanced chemical vapor deposition (PECVD), low pressure chemical vapor deposition (LPCVD), metal organic chemical vapor deposition (MOCVD), atomic layer deposition (ALD), plasma enhanced atomic layer deposition (PEALD), or through direct metal deposition (DMD), etc. These examples are not intended to be limiting. Certain disclosed embodiments may be useful whenever wafer stress and/or bowing are induced due to material

present on the frontside of the wafer.

[0031] The frontside stacks may be deposited to any number of layers and thicknesses. In an example, the stack includes about 20 or more layers, and has a total thickness of about 2 μm to about 4 μm. However, in some cases, multiple-layer stacks have about one hundred or more layers. In some embodiments, multiple-layer stacks may have about five hundred or more layers. In some embodiments, the multiple-layer stacks may have about one thousand or more layers. Such stacks may have a thickness of about 4 μm to 12 μm, for example.

[0032] The stress induced in the wafer by the stack or other frontside deposition may be about −500 MPa to about +500 MPa. In some embodiments, the resulting in a bow is about 150 μm or greater, e.g., about 300 μm and above, about 400 μm and above, or about 200 μm to about 400 μm (for a 300 mm wafer).

[0033] Another cause of wafer bow may be frontside processing which uses thick hardmasks with limited etch selectivity. In these embodiments, at least one of the one or more frontside layers is a hardmask. The thick hardmasks may have an internal stress similar to those described above, e.g., have a magnitude of 0 MPa to about 500 MPa. The stress caused by the hardmask may be tensile stress or compressive. The thick hardmasks may cause wafers to have a significant wafer bow, e.g., about 150 μm or more.

[0034] Various techniques have been devised for combatting bowing. When bowing is more severe, deposition processes may be tuned to reduce or counteract internal stresses in deposited layers. However, any such tuning should not interfere with process requirements for fabricating devices. One commonly used technique to counteract bowing deposits a film on the back side of the wafer.

[0035] Backside deposition may form a high-stress film. If the backside layer has the same type of internal stress (tensile or compressive) and of comparable magnitude to the internal stress created on the frontside, the backside film effectively counteracts and reduces the bow.

[0036] Examples of backside films used to counteract bow include the following: amorphous silicon, silicon oxide, silicon nitride, and silicon oxynitride. Current backside films have high internal stress and can mitigate the stresses imparted on the wafer from the frontside layers to reduce or eliminate the wafer bow. Generally, backside layers are made of films with high stress.

[0037] Until relatively recently, the backside film thickness remained relatively thin (e.g., <1um) because the bow caused by depositing material on the frontside was relatively modest. Thus, downstream processes at previous technology nodes did not normally experience issues addressed by embodiments herein. However, modern IC fabrication techniques may produce

substrates having frontside layers that produce much more severe wafer bow compared to previous nodes. For example, some modern processes use thick hardmask layers in operations where the etch selectivity between the hardmask and etched material is limited, yet deep trenches or vias are etched. In another example, frontside stacks have increased the number of layers. For example, in previous nodes stacks may have been about 32 to about 72 layers. Now, stacks may have hundreds or even thousands of layers, increasing the thickness of the frontside layer and the internal stress. Typically wafer bow compensation is achieved by depositing a single backside layer. Due to the increasing magnitude of wafer bow, thicker backside films must be deposited to compensate for wafer bow. This has caused certain issues. Due to large internal forces occurring within thick backside layers, the layers may spontaneously form film cracks. For many film materials (e.g., tensile silicon nitride films), cracks are observed in films of thicknesses necessary to compensate for bow values above a critical bow limit. These bow limits are commonly known as the "bow cracking limit" or "cracking margin."

[0038] In some embodiments, the internal stress of frontside layers, and bowing of the substrate may also change when heated from room temperature to processing temperatures, including temperatures that may be used for annealing films e.g., temperatures greater than about 400 °C, 450 °C, 500°C, 550°C, 600°C, or 650°C. This change may result from differences in the thermal expansion coefficient of the substrate vs the frontside layers. For example, if the wafer, which is silicon, has a greater thermal expansion coefficient than the frontside layers, which may be oxide and/or nitride layers, then upon heating the difference in expansion between the wafer and the frontside layers may cause a tensile stress shift of the frontside layers that results in a corresponding dynamic wafer bow. Even if the wafer bow is substantially neutral at ambient temperature, wafer bow at elevated temperatures may negatively affect processing for reasons outlined above.

[0039] The thermal stress shift of frontside layers may be compensated by depositing backside layers that have a similar thermal stress shift to the frontside layers, and thus provide a dynamic wafer bow compensation upon heating. However, as the thickness and corresponding internal stress of frontside layers increases, the thickness of backside layers must also increase to compensate the greater internal stress and greater thermal stress shifts. However, greater thicknesses increases the risks of cracks, improper clamping by an electrostatic chuck, inability to be held by a wafer handler, pattern transfer issues during photolithography issues, and other undesirable effects.

BACKSIDE FILM INTERNAL STRESS SHIFT COMPENSATION

[0040] Disclosed herein are methods, systems, and techniques for compensating internal stress shift of frontside layers with backside layers that have a similar stress shift upon heating. This reduces the need for additional backside film deposition, reduces the risk of a wafer handling problem during subsequent wafer processing, and maintains wafer bow compensation after annealing without cracking of the backside films.

[0041] As noted above, thermal stress shifts may result from a difference between the thermal expansion coefficient of the substrate and various layers deposited on the frontside and backside of the substrate. Generally, the bulk of the wafer comprises silicon that has a higher CTE than frontside layers such as an ONON stack. Thus, upon heating, the silicon expands more than the ONON layers, resulting in a tensile thermal stress shift. The magnitude of the thermal stress shift depends on the difference in the CTE between the silicon wafer and the frontside layers, as a greater difference will cause a greater thermal stress shift. Notably, the CTE of the silicon wafer and frontside layers may both be positive, but the CTE of the silicon wafer is greater than the CTE of the frontside layers, resulting in a thermal stress shift.

[0042] Frontside layers may undergo a thermal stress shift that may be compensated by backside layers that undergo a similar thermal stress shift. However, as the thickness of the frontside layers increases, the thickness of the backside layers may similarly need to increase to properly compensate the frontside layers, particularly as the backside layers may have a similar composition as the frontside layers (e.g., silicon nitride or silicon oxide). As the composition of frontside and backside layers may be similar, the CTE and corresponding thermal stress shifts may also be similar.

[0043] Disclosed herein are methods, systems, and devices that utilize a backside layer having a negative thermal expansion coefficient (NTE). NTE materials may include mixed metal oxides of Silicon, Scandium, Tungsten, Zirconium, or any combinations thereof. In some embodiments the mixed metal oxides may also have dopants, e.g., doped silicon oxide. A negative NTE will have a greater difference between the CTE of the NTE material and the CTE of the wafer than a silicon oxide or silicon nitride films, which both have positive CTE. Thus, a NTE layer will have a greater stress shift at a given thickness than a positive CTE layer. This greater stress shift allows the backside layer to be thinner while compensating the same amount of thermal stress shift.

[0044] Figures 2A and 2B show flowcharts that illustrates example sequences of operations to reduce substrate bow.

[0045] In Figure 2A, at 202, operation (A) to determine how wafer bow changes as a function

of temperature applied to the wafer can be performed. To determine or estimate wafer bow, and particularly wafer bow as a function of temperature, various metrology and/or analytical techniques may be employed. In certain embodiments, to determine wafer bow, a test wafer may be employed. The test wafer may have some front or active side processing performed and the bow reflects internal stresses caused by that front side processing. In some embodiments, a goal of the process is to determine back side processing that compensates for the bowing resulting from internal stresses caused by one or more front side processes. Therefore, the test wafer may be fully or partially processed in accordance with the front side processing that is to be compensated for. As an example, a test wafer may have a fully or partially deposited stack including alternating layers of silicon oxide and silicon nitride (ONON) on the front or active side of a semiconductor wafer.

[0046] Certain front side processes produce temperature variations on the wafer. For example, some processes are performed at elevated temperatures (e.g., about 300°C or higher). A production wafer may be stored at room temperature (e.g., in a front-opening universal pod or FOUP) waiting in a queue of wafers to be processed. When the wafer is delivered to a process chamber where the elevated temperature process is to be performed, the wafer is heated. After processing is complete, the wafer may be cooled by, for example, removal from the process chamber. This heating-processing-cooling process may introduce a sequence of bowing that culminates in bow to the wafer that has been fully processed.

[0047] To design a back side treatment (e.g., depositing one or more back layers) that accounts for the bow variations experienced by production wafers during a particular process or group of processes that involve temperature variations, the test wafer may be evaluated at multiple temperatures within or overlapping with the range of temperatures experienced by a production wafer in processes that introduce bow.

[0048] In certain embodiments, the test wafer is exposed to at least two or more different temperatures within or overlapping with the range of temperatures experienced by a production wafer in processes that introduce bow. In certain embodiments, the test wafer is exposed to a range of temperatures that cover less than about 50% of the range of temperatures experienced by a production wafer in processes that introduce bow. In certain embodiments, the test wafer is exposed to a range of temperatures that cover at least about 50% of the range of temperatures experienced by a production wafer in processes that introduce bow. In certain embodiments, the test wafer is exposed to a range of temperatures that cover about 80% of the range of temperatures experienced by a production wafer in processes that introduce bow. In certain embodiments, the test wafer is exposed to a range of temperatures that include at least the range about 50°C to about

400°C. In certain embodiments, the test wafer is exposed to a range of temperatures that include at least the range about 30°C to about 500°C.

[0049] In certain embodiments, the test wafer is exposed to a sequence of two more temperatures of increasing temperature, and the same test wafer is exposed to a sequence of two more temperatures of decreasing temperature. In this way, bow versus temperature hysteresis may be measured.

[0050] Wafer bow may be measured by various techniques. One example is low coherence laser interferometry utilizing a Michelson interferometer with a low coherence light source such as one or more components of the 413 Series Thickness and Total Variation (TTV) mapping system sold by the Frontier Semiconductor Company located at 165 Topaz St., Milpitas, CA 95035. Such equipment can measure substrate thickness, warp, and TTV, with or without Tape, for Wafer Backgrind and Etch Thinning processes. In certain embodiments, bow is not measured directly or a surrogate for bow is measured. For example, the internal stress, which gives rise to bow and results from front side processing, is measured.

[0051] At 204, operation (B) that uses information about how the determined wafer bow changes as a function of temperature to determine properties of the back side treatment can be performed. The bow versus temperature response of a wafer contains information that allows design of a back side treatment that counteracts the wafer bow over a range of temperatures associated with front side processing.

[0052] Various back side processes may be employed. Examples include deposition of one or more layers, etching (wet or dry), implantation/doping, and exposure to plasma. The process may identify any one or more of these types of back side processes to counteract temperature-dependent bowing in one or more front side processes.

[0053] In various embodiments, determining a back side treatment to counteract bowing employs temperature-dependent information about one or more optional back side treatments. For example, the determination may employ data about how a test wafer with a layer of one material (e.g., zirconium tungstenate) bows with different temperatures. In some cases, the determination may employ data about how two different test wafers each with a different layer of material (e.g., silicon oxide and silicon nitride) bow with different temperatures. In another example, the determination may employ data about how a test wafer with some material etched away (or exposed to plasma) bows with different temperatures. In another example, a first test wafer may include a material having a negative thermal expansion coefficient on its back side. In another example, a first test wafer may include a first material (e.g., silicon nitride) on its back side and a

second wafer may include a deposited layer of a second material (e.g., silicon oxide) on its back side.

[0054] In certain embodiments, one or more test wafers having the optional back side treatments are exposed to a range of temperatures that substantially tracks the range of temperatures experienced by a production wafer in processes that introduce bow (i.e., the processes that the back side processing will compensate for). In certain embodiments, one or more test wafers having the optional back side treatments are exposed to a range of temperatures that substantially tracks the range of temperatures that a different test wafer is exposed for purposes of generating the bow versus temperature information for front side processing (e.g., operation (A) discussed above).

[0055] Various analytical techniques may be employed to determine a back side treatment to be applied to production wafers to counteract bowing caused by the one or more processes performed on a front side of a wafer. For example, a technique may compare the bow caused by the one or more processes at various temperatures against the bow caused by each of multiple optional back side processes at the various temperatures. In this way, a composite back side process can be determined that accounts for bowing over a range of temperatures. In certain embodiments, this temperature dependent comparison can be accomplished implicitly, as by a machine learning technique, for example.

[0056] It should be apparent that, in some embodiments, a determined back side treatment is a composite of two or more optional/unitary back side processes. In one example, the back side treatment includes depositing two or more layers on top of one another. In certain embodiments, these layers are different materials disclosed herein.

[0057] At 206, operation (C) to apply the back side treatment identified in (B) to an incoming wafer (e.g., a production wafer) can be performed. In certain embodiments, the same back side treatment is performed on a batch of wafers or multiple batches of wafers, without re-determining an appropriately compensating back side treatment. In some embodiments, the same back side treatment is performed on all wafers subject to a defined process (or process sequence) for which the back side treatment was determined. The back side treatment applied to production wafers at least partially prevent those wafers from bowing in response to the front side processes.

[0058] At 208, operation (D) to perform the one or more processes on the front side of the incoming wafer can be performed.

[0059] When a front side process parameter changes (for a production process), a compensating back side treatment may be re-determined via operations (A) and (B) as discussed above. In this case, at least the bow versus temperature information for the new or modified front side processing

is generated. The resulting new information is applied in operation (B) to determine a new back side treatment.

[0060] In some examples, the back side treatment is determined using (i) bow metrology on test wafers that have undergone front side processing corresponding to a production process, (ii) bow metrology on different test wafers that have undergone different optional back side treatments that might counteract bow induced by the front side processing, (iii) and an analytical technique that compares temperature-dependent bowing obtained via (i) and (ii). This process may be conducted infrequently, for example, whenever a front side process parameter changes, a new process chamber is used, or some other change to the production process occurs.

[0061] In certain embodiments, both active side and back side processing may be achieved utilizing one or more RF signals, which may operate to generate a plasma, which may bring about or enhance particular wafer fabrication processes. Active side and back side processing may be affected by the RF power coupled to a fabrication chamber, the frequency of the RF signal that brings about formation of the plasma, the exposure time of the plasma, temperature of the substrate and reaction chamber, pressure within the reaction chamber, flow of inert gas, composition of reactants, etc. as the high frequency (HF, e.g., about 13.5 MHz, or about 27.0 MHz, for example) component of the RF power used to generate the plasma increases, the tensile stress response of the film may also increase, while the compressive stress response shows substantially no change. Example HF RF powers may range between about 0-2500 Watts per station of a multi-station fabrication chamber. As the low frequency (LF, e.g., about 356 kHz, about 400 kHz, etc.) component of the RF power used to generate the plasma increases, the tensile stress response of the film may decrease, and the compressive stress response of the film may increase. Example LF RF frequencies may range between about 200 KHz-4MHz. Example LF powers may range between about 0-2500 Watts per station. In various cases, the LF + HF powers together may range between about 0-2500 Watts per station. As the plasma exposure time and/or duty cycle increases, the stress response may change as indicated above depending on the frequency used and the type of film stress involved. Example RF exposure times depend on the type of deposition occurring. For instance, plasma enhanced chemical vapor deposition involves exposure to plasma for relatively long periods of time, while plasma enhanced atomic layer deposition involves repeated exposure to plasma for much shorter periods of time. As the temperature of the substrate during deposition increases, both the tensile and compressive stress responses of the film increase. Example substrate and chamber temperatures also depend on the deposition process, but may be between about 25°C to about 650°C. As the pressure in the reaction chamber during deposition increases, the tensile stress response of the film increases, and the compressive stress response of

the film may decrease. Example chamber pressures range between about 1-4 Torr. As the inert gas flow delivered to the reaction chamber during deposition increases, the tensile stress response shows no change, and the compressive stress response increases. Example flow rates for inert gas may be between about 100-5000 sccm. Another parameter that may affect film stress is the electrode spacing. The electrode spacing is important because it affects the E-field on the wafer, which can affect on-film density. As the electrode spacing increases, there is no response in the tensile stress response, and the compressive stress response decreases. Example electrode spacing may be between about 5-30mm. Other reaction parameters related to back side deposition will be further discussed below.

[0062] Another variable that can affect the degree of stress in a film is the hydrogen content of the film which can be controlled by the flow of NH_3 or other hydrogen-containing reactant. One or more of the variables discussed above may also directly or indirectly affect the hydrogen content of the film.

[0063] As mentioned, stacks of deposited materials are especially likely to result in wafer stress and bowing. One example stack that may cause these problems is a stack having alternating layers of oxide and nitride (e.g., silicon oxide/silicon nitride/silicon oxide/silicon nitride (ONON), etc.). Another example stack likely to result in bowing includes alternating layers of oxide and polysilicon (e.g., silicon oxide/polysilicon/silicon oxide/polysilicon, etc.). Other examples of stack materials that may be problematic include, but are not limited to, tungsten and titanium nitride. The materials in the stacks may be deposited through chemical vapor deposition techniques such as plasma enhanced chemical vapor deposition (PECVD), low pressure chemical vapor deposition (LPCVD), metal organic chemical vapor deposition (MOCVD), atomic layer deposition (ALD), plasma enhanced atomic layer deposition (PEALD), or through direct metal deposition (DMD), etc. These examples are not intended to be limiting. Certain disclosed embodiments may be useful whenever wafer stress and/or bowing are induced due to material present on the active side of the wafer.

[0064] The active side stacks may be deposited to any number of layers and thicknesses. In a typical example, the stack includes between about 32-72 layers, and has a total thickness between about 2-4 μm. The stress induced in the wafer by the stack may be between about -500 MPa to about +500 MPa, resulting in a bow that is frequently between about 200-400 μm (for a 300 mm wafer), and even greater in some cases.

[0065] Figure 2B shows an example process of deposition of a backside layer structure including a backside layer having a negative coefficient of thermal expansion. The process of Figure 2B

starts with receiving a substrate having one or more frontside layers having a tensile stress shift (212). The wafer may have one or more frontside layers deposited thereon that cause bowing of the wafer.

[0066] One or more first backside layers having a NTE are deposited onto the wafer (214). In some embodiments, the internal stress of the first backside layer may counteract the internal stress from the frontside layer and may help reduce wafer bow. In other embodiments, the first backside layer may have a relatively neutral internal stress at ambient temperature and not compensate any wafer bow caused by the frontside layers at ambient temperatures. The first backside layers may have a tensile stress shift, i.e., under heating conditions the internal stress of the layer may increase (become more tensile). In some embodiments, the first backside layers may be a NTE material and may not compensate internal stress from the frontside layers at ambient temperature. For example, the backside layer may have a relatively neutral stress at ambient temperature, but will undergo a thermal stress shift to counteract the thermal stress shift of the frontside layers.

[0067] The thickness of the NTE layers may be based upon the dynamic wafer bow caused by the frontside layers if untreated. This dynamic wafer bow may be determined as described above. As the NTE has a larger thermal stress shift than the frontside layers, an NTE layer may be relatively thin. In some embodiments, a NTE layer may compensate dynamic wafer bow at a rate of at least about 0.5 μm of dynamic wafer bow / 1 μm of thickness of the NTE layer / °C. Thus, to compensate a dynamic wafer bow of 450 μm over a temperature difference of 550 °C, an NTE layer of at least about 1.6 μm may be used. This may be substantially thinner than silicon oxide and/or silicon nitride backside layers, which may require a thickness of at least about 4 μm to compensate the same amount of dynamic wafer bow, e.g., a compensation of dynamic wafer bow of about 0.2 μm dynamic wafer bow / 1 μm of thickness / °C.

[0068] In an optional embodiment, one or more second backside layers are deposited having an internal stress that compensates an internal stress of the one or more frontside layers (216). The second backside layers may have an internal stress that is the same as the internal stress of the frontside layer at ambient temperatures. Thus, the second backside layers may compensate wafer bow caused by the frontside layers at ambient temperature and the first backside layers compensate dynamic wafer bow resulting from thermal stress shift. In some embodiments, the second backside layers may also undergo a thermal stress shift, which may be considered when determining the properties of the first backside layers, e.g., the total thickness of the first backside layer. In other embodiments, the first backside layer compensates substantially all of the dynamic wafer bow caused by the frontside layers.

[0069] After deposition of the backside layers, the substrate may undergo a fabrication operation at a temperature that causes the front and backside layers to have a thermal stress shift. (218). While the frontside layers and the backside layers may individually experience a thermal stress shift, the combined internal stress from both films remains substantially the same, e.g., the internal stress of the combined frontside layers and backside layers changes by less than about 10%, less than about 5%, less than about 2%, or less than about 1%.

[0070] The backside layers may be deposited using CVD, PECVD, ALD, epitaxy, PVD, or other deposition processes. The backside layers may be deposited using a special purpose backside deposition apparatus. The backside deposition apparatus may be a different deposition apparatus then the apparatus used to deposit the one or more frontside layers.

[0071] The bow induced by the backside layers may be the sum of the individual induced bows. In some embodiments, bow magnitude of the combined backside layers may be about the same as the bow magnitude of the one or more frontside layers. In some embodiments, the bow contributions of all frontside and backside layers may combine so that the total bow of the wafer is minimal (i.e., less than about 100 μm.) In some embodiments, after performing the method of Figure 2A or 2B, the wafer may be substantially flat, e.g., the wafer has a bow of about 200 μm or less, about 150 μm or less, or about 100 μm or less. In some embodiments, the wafer may stay substantially flat at temperatures between ambient and about 700°C.

[0072] Note that references to bow values induced or caused by individual backside layers assume that the bow is uncompensated by other layers. For example, when referring to the magnitude of a bow caused by a first backside layer, we assume that is the bow that would be produced on the substrate if no other layers were present, e.g., no frontside layers. The magnitude of a bow induced by a layer depends on both the internal stress of the material in the layer and the thickness of the layer.

[0073] Compensation by backside layers refers to bow contributions of backside layers that may combine with bow contributions of frontside layers to reduce or equalize wafer bow. As noted above, bow contributions of all frontside and backside layers may be combined. A positive bow caused by frontside layers, forming a bowl shape, may be caused by frontside layers having a tensile internal stress. This bow may be reduced by a backside layer also having a tensile internal stress that causes an opposite, negative bow. The negative bow caused by the backside layer compensates the positive bow caused by the frontside layers, resulting in a total bow of the wafer that is minimal. In some embodiments, compensation may include partially mitigating wafer bow. As noted above, a NTE backside layer may compensate wafer bow at elevated temperatures, e.g.,

compensate dynamic wafer bow caused by thermal stress shifts of the frontside layers. In some embodiments, a NTE backside layer may also compensate wafer bow at ambient conditions. In some embodiments, a NTE backside layer may not compensate wafer bow at ambient conditions. In other embodiments, backside layers may fully compensate wafer bow, e.g., reduce wafer bow to less than about 100 μm. In some embodiments, an NTE layer may have a slightly compressive stress at room temperature, but have a thermal stress shift that is positive, i.e., more tensile.

[0074] In certain embodiments, a backside layer disclosed herein comprise a material having an intrinsic internal stress, which has a magnitude of at least about 100 MPa or about 100 to about 2000 MPa. These values may be for tensile or compressive internal stress, as the case may be for the type of backside material needed to counteract bow caused by the frontside layer(s). The above-recited internal stress values may apply to any one or more backside layers in a multilayer backside stack. Any two backside layers may have the same or different values of internal stress.

[0075] Example materials used to make backside layers having tensile internal stress include mixed metal oxides (e.g., oxides of Scandium, Tungsten, Zirconium, or any combinations thereof), silicon nitrides (SiN), silicon oxynitrides, and polymer layers. As examples, tensile films can be deposited using PVD, CVD, or PECVD techniques. To combat wafer bow caused by a frontside layer with a compressive internal force, a compressive film may be used for the bulk backside layers. Compressive films may be formed using specific materials and/or processing conditions. Example materials used to make compressive films include silicon oxides (SiO_x), silicon nitrides, aluminum oxides, aluminum nitrides, and polysilicon. Compressive films can be deposited using CVD or PECVD techniques. The above-recited materials and deposition techniques may apply to any one or more backside layers in a multilayer backside stack. Any two backside layers may be formed by the same or different techniques.

[0076] NTE backside films disclosed herein may be deposited using PVD techniques using metal-containing reactants and oxygen-containing reactants. In some embodiments, a PLD technique may be used wherein a laser vaporizes a source material in the presence of oxygen to deposit a metal oxide film having a NTE. The properties of a NTE backside film may also be tuned by control of various process parameters. Such process parameters may include temperature, pressure, species flow rates, plasma power, etc.

[0077] Backside films disclosed herein may be deposited using PECVD techniques using silicon-containing precursors and nitrogen-containing reactants. The internal stress shift of films may be tuned to either tensile or compressive, and the magnitude of such shifts may also be tuned by control of various process parameters. Such process parameters may include temperature,

pressure, species flow rates, plasma power, etc.

[0078] Mixed metal films, e.g., Scandium, Tungsten, Zirconium, or any combinations thereof, may be deposited by sputtering processes. For depositing sputtered films, a source of the film to be deposited is provided in a process chamber and may be sputtered by various methods to cause a vapor stream of the composition, which may then deposit on the substrate. For example, a source of zirconium tungstenate may be provided into a process chamber and sputtered to deposit a film of zirconium tungstenate as a PVD process.

[0079] For depositing silicon-containing films, one or more silicon-containing precursors may be used. In some examples, silicon-containing precursors can include silanes (e.g., SiH_4), polysilanes ($H_3Si\text{-}(SiH_2)_n\text{-}SiH_3$) where $n \geq 1$, organosilanes, halogenated silanes, aminosilanes, alkoxysilanes, and the like. Organosilanes such as methylsilane, ethylsilane, isopropylsilane, t-butylsilane, dimethylsilane, diethylsilane, di-t-butylsilane, allylsilane, *sec*-butylsilane, thexylsilane, isoamylsilane, t-butyldisilane, di-t-butyldisilane, and the like.

[0080] A halosilane includes at least one halogen group and may or may not include hydrogens and/or carbon groups. Examples of halosilanes are iodosilanes, bromosilanes, chlorosilanes, and fluorosilanes. Specific chlorosilanes are tetrachlorosilane, trichlorosilane, dichlorosilane, monochlorosilane, chloroallylsilane, chloromethylsilane, dichloromethylsilane, chlorodimethylsilane, chloroethylsilane, t-butylchlorosilane, di-t-butylchlorosilane, chloroisopropylsilane, chloro-sec-butylsilane, t-butyldimethylchlorosilane, thexyldimethylchlorosilane, and the like.

[0081] An aminosilane includes at least one nitrogen atom bonded to a silicon atom, but may also contain hydrogens, oxygens, halogens, and carbons. Examples of aminosilanes are mono-, di-, tri- and tetra-aminosilane ($H_3Si(NH_2)$, $H_2Si(NH_2)_2$, $HSi(NH_2)_3$ and $Si(NH_2)_4$, respectively), as well as substituted mono-, di-, tri- and tetra-aminosilanes, for example, t-butylaminosilane, methylaminosilane, tert-butylsilanamine, bis(tert-butylamino)silane ($SiH_2(NHC(CH_3)_3)_2$ (BTBAS), tert-butyl silylcarbamate, $SiH(CH_3)\text{-}(N(CH_3)_2)_2$, $SiHCl\text{-}(N(CH_3)_2)_2$, $(Si(CH_3)_2NH)_3$, di-isopropylaminosilane (DIPAS), di-sec-butylaminosilane (DSBAS), $SiH_2[N(CH_2CH_3)_2]_2$ (BDEAS) and the like. A further example of an aminosilane is trisilylamine ($N(SiH_3)$). In some embodiments, an aminosilane that has two or more amine groups attached to the central Si atom may be used. These may result in less damage than aminosilanes having only a single amine group attached.

[0082] Further examples of silicon-containing precursors include trimethylsilane (3MS); ethylsilane; butasilanes; pentasilanes; octasilanes; heptasilane; hexasilane; cyclobutasilane;

cycloheptasilane; cyclohexasilane; cyclooctasilane; cyclopentasilane; 1,4-dioxa-2,3,5,6-tetrasilacyclohexane; diethoxymethylsilane (DEMS); diethoxysilane (DES); dimethoxymethylsilane; dimethoxysilane (DMOS); methyl-diethoxysilane (MDES); methyl-dimethoxysilane (MDMS); octamethoxydodecasiloxane (OMODDS); tert-butoxydisilane; tetramethylcyclotetrasiloxane (TMCTS); tetraoxymethylcyclotetrasiloxane (TOMCTS); triethoxysilane (TES); triethoxysiloxane (TRIES); and trimethoxysilane (TMS or TriMOS).

[0083] In some implementations silicon-containing precursors may include siloxanes or amino-group-containing siloxanes. In some embodiments, siloxanes used herein may have a formula of $X(R^1)_aSi\text{-}O\text{-}Si(R^2)_bY$, where a and b are integers from 0 to 2, and X and Y independently can be H or NR^3R^4, where each of R1, R2, R3 and R4 is hydrogen, unbranched alkyl, branched alkyl, saturated heterocyclic, unsaturated heterocyclic groups, or combinations thereof. In some embodiments, when at least one X or Y is NR^3R^4, R3 and R4, taken together with the atom to which each are attached, form a saturated heterocyclic compound. In some embodiments, the silicon-containing precursors are pentamethylated amino group containing siloxanes or dimethylated amino group containing siloxanes. Examples of amino group containing siloxanes include: 1-diethylamino 1,1,3,3,3,-pentamethyl disiloxane, 1-diisopropylamino-1,1,3,3,3,-pentamethyl disiloxane, 1 dipropylamino-1,1,3,3,3,-pentamethyl disiloxane, 1-di-n-butylamino-1,1,3,3,3,-pentamethyl disiloxane, 1-di-sec-butylamino-1,1,3,3,3,-pentamethyl disiloxane, 1-N-methylethylamino 1,1,3,3,3,-pentamethyl disiloxane, 1-N-methylpropylamino-1,1,3,3,3,-pentamethyl disiloxane, 1 N-methylbutylamino -1,1,3,3,3,-pentamethyl disiloxane, 1-t-butylamino -1,1,3,3,3,-pentamethyl disiloxane, 1-piperidino-1,1,3,3,3,-pentamethyl disiloxane, 1-dimethylamino-1,1-dimethyl disiloxane, 1-diethylamino-1,1-dimethyl disiloxane, 1-diisopropylamino-1,1-dimethyl disiloxane, 1-dipropylamino-1,1-dimethyl disiloxane, 1-di-n-butylamino-1,1-dimethyl disiloxane, 1-di-sec butylamino-1,1-dimethyl disiloxane, 1-N-methylethylamino-1,1-dimethyl disiloxane, 1-N methylpropylamino-1,1-dimethyl disiloxan,e 1-N-methylbutylamino -1,1-dimethyl disiloxane, 1 piperidino-1,1-dimethyl disiloxane, 1-t-butylamino -1,1-dimethyl disiloxane, 1-dimethylamino- disiloxane, 1-diethylamino- disiloxane, 1-diisopropylamino- disiloxane, 1-dipropylamino- disiloxane, 1-di-n-butylamino- disiloxane, 1-di-sec-butylamino- disiloxane, 1-N methylethylamino- disiloxane, 1-N-methylpropylamino-disiloxane, 1-N-methylbutylamino – disiloxane, 1-piperidino- disiloxane, 1-t-butylamino disiloxane, and 1-dimethylamino-1,1,5,5,5,-pentamethyl disiloxane.

[0084] Where a deposited film includes nitrogen, a nitrogen-containing reactant may be used. A nitrogen-containing reactant contains at least one nitrogen, for example, nitrogen (N_2), ammonia (NH_3), hydrazine (N_2H_4), amines (e.g., amines bearing carbon) such as methylamine (CH_5N),

dimethylamine ($(CH_3)_2NH$), ethylamine ($C_2H_5NH_2$), isopropylamine (C_3H_9N), t-butylamine ($C_4H_{11}N$), di-t-butylamine ($C_8H_{19}N$), cyclopropylamine ($C_3H_5NH_2$), sec-butylamine ($C_4H_{11}N$), cyclobutylamine ($C_4H_7NH_2$), isoamylamine ($C_5H_{13}N$), 2-methylbutan-2-amine ($C_5H_{13}N$), trimethylamine (C_3H_9N), diisopropylamine ($C_6H_{15}N$), diethylisopropylamine ($C_7H_{17}N$), di-t-butylhydrazine ($C_8H_{20}N_2$), as well as aromatic containing amines such as anilines, pyridines, and benzylamines. Amines may be primary, secondary, tertiary or quaternary (for example, tetraalkylammonium compounds). A nitrogen-containing reactant can contain heteroatoms other than nitrogen, for example, hydroxylamine, t-butyloxycarbonyl amine and N-t-butyl hydroxylamine are nitrogen-containing reactants. Other examples include N_xO_y compounds such as nitrous oxide (N_2O), nitric oxide (NO), nitrogen dioxide (NO_2), dinitrogen trioxide (N_2O_3), dinitrogen tetroxide (N_2O_4) and/or dinitrogen pentoxide (N_2O_5).

[0085] Figures 3A and 3B illustrate backside layers having tensile stress shifts wherein one backside layer is a NTE material. In Figure 3A, a substrate 300 has a backside layer 215a having a tensile thermal stress shift. The substrate is relatively flat at ambient temperature. Upon heating, the substrate and backside layer bow into substrate 300b and backside layer 315b. Then, upon cooling, the substrate and backside layer have a corresponding thermal stress shift back to a neutral stress and relatively flat shape.

[0086] Figure 3B is similar to Figure 3A, however backside layer 317a is a NTE that is substantially thinner than backside layer 315a. The substrate is relative flat at ambient temperature. Upon heating, the substrate and backside layer bow into substrate 300b and backside layer 317b. Then, upon cooling, the substrate and backside layer have a corresponding thermal stress shift back to a neutral stress and relatively flat shape. Notably, the bowing caused by backside layer 317b is the same amount as the bowing caused by backside layer 315b, but backside layer 317b is much thinner. In some embodiments, backside layer 315a, which may comprise silicon nitride or silicon oxide, may have a thickness of about 4-5 μm, while backside layer 317b may have a thickness of less than about 2 μm while causing the same amount of wafer bow.

[0087] Figures 4A-C illustrate bowing of a substrate having a frontside layer and backside layers having thermal stress shifts. Figure 4A illustrates a substrate 400 having frontside layers 411a. Upon heating to a high temperature, e.g., temperatures greater than about 400 °C, 450°C, 500°C, 550°C, 600°C, or 650°C, frontside layers 411a undergo a thermal stress shift that results in bowed frontside layers 411b and bowed substrate 400a.

[0088] Figure 4B illustrates substrate 400 having backside layers 415a comprising silicon oxide and/or silicon nitride. Upon heating to a high temperature, the substrate remains relatively flat, as

shown by substrate 400b, frontside layers 411c, and backside layers 415b. While the backside layers 415a/b compensate the thermal stress shift of frontside layers 411a/c, the thickness of the backside layers 415a/b is similar to the thickness of frontside layers 441a/c. In some embodiments the thickness of backside layers 415a/b may be about 4-5 μm to compensate a 450 μm dynamic wafer bow.

[0089] Figure 4C illustrates substrate 400 having backside layers 417a comprising a NTE material. Upon heating to a high temperature, the substrate remains relatively flat, as shown by substrate 400b, frontside layers 411c, and backside layers 417b. The backside layers 417a/b compensate the thermal stress shift of frontside layers 411a/c with a much thinner film than backside layers 415a/b. In some embodiments the thickness of backside layers 415a/b may be about 2 μm or between about 1 and about 2 μm to compensate a 450 μm dynamic wafer bow. Thicker backside layers may be used to compensate greater dynamic wafer bow on a substantially linear relationship.

[0090] Figure 5 is a chart showing an estimate of wafer bowing for oxide/nitride layers (ONON), a NTE layer, and combined layers (e.g., layers including ONON frontside layers and a NTE backside layer). As shown in Figure 4, ONON layers have a negative bow from about 25°C to about 450°C, crossing from negative to positive values of bowing. Bowing from a NTE layer is also shown. As previously described, by adjusting the thickness of the NTE layer wafer bowing may be controlled over various temperatures. The chart of Figure 5 may be an example of compensating wafer bow as shown in Figure 4C, i.e., a relatively thin NTE backside layer compensating a larger amount of dynamic wafer bow. Wafer bow is generally a function of internal stress of a film and the thickness of the film. For dynamic wafer bow, the CTE of the film is also relevant, as a larger difference between the CTE of the substrate, e.g., silicon, and the layers will result in a larger stress shift per °C. For NTE materials, the difference in CTE between the NTE material and the silicon wafer is much larger than the difference in CTE between silicon nitride/oxide and the silicon wafer. Thus, the thermal stress shift of an NTE material will be much larger.

[0091] Thus, in the instance of Figure 5, if oxide/nitride (ONON) present on an active side of a semiconductor wafer is combined with a proper thickness of an NTE layer at the back side of the wafer, bowing of the semiconductor wafer can be controlled. Accordingly, as is also shown in Figure 4, when (ONON) is combined with a layer of NTE material ("combined" in Figure 5) the contributions of active side and back side layers sum to a nominal value, that approaches 0. In particular implementations, some amount of bowing of a semiconductor wafer may be tolerable, such as a bowing of, for example, 10 μm, 20 μm, 30 μm, 40 μm, 50 μm, 60 μm, 70 μm, 80 μm,

90 μm, 100 μm, or more. If bowing of a semiconductor wafer remains below one of the aforementioned tolerances, subsequent semiconductor processes, such as photolithography, die singulation, or the like, may be unaffected.

[0092] In some embodiments, the NTE material may have an internal stress at ambient temperature that corresponds to an internal stress of frontside layers at ambient temperature. In other embodiments, the NTE material may have a substantially neutral internal stress at ambient temperature and a large thermals tress shift. In some embodiments, an NTE layer may have a slightly compressive stress at room temperature, but have a thermal stress shift that is positive, i.e., more tensile. In such embodiments, a first backside layer may be deposited that compensates for wafer bow at ambient temperature. A second backside layer including a NTE material may be deposited and thus compensate for dynamic wafer bow. In some embodiments, the NTE material does not compensate internal stress at ambient temperatures.

[0093] In some embodiments, the frontside layers may have a tensile internal stress at room temperature while a backside layer of an NTE material has a compressive internal stress. In such embodiments, an additional backside layer may compensate wafer bow at ambient temperatures, including wafer bow caused by the NTE material, while the NTE layer compensates dynamic wafer bow.

Apparatus

[0094] In some embodiments, FIG. 6A is a block diagram that illustrates a substrate processing system 600 used to perform processing on a wafer 602 (also referred to as a wafer), according to some embodiments. As shown, the substrate processing system may include a chamber 634. A center column may be configured to support a pedestal for when a top surface of the wafer 602 is being processed, e.g., a film is being formed on the top surface of the wafer 602, or on the backside of the wafer 602. The pedestal, in accordance with some embodiments disclosed herein, may be referred to as a showerhead-pedestal ("ShoPed") 606. A showerhead 636 may be disposed over the ShoPed 606.

[0095] In some embodiments, the showerhead 636 may be electrically coupled to power supply 638 via a match network 640. The power supply 638 may be controlled by a control module 642, e.g., a controller. In some embodiments, power may be provided to the ShoPed 606 instead of the showerhead 636. The control module 642 may be configured to operate the substrate processing system 632 by executing process input and control for specific process recipes. Depending on whether the top surface of the wafer 602 is receiving a deposited layer or layer stack or the bottom surface of the wafer 602 is receiving a deposited layer or layer stack, the controller module 642

may set various operational inputs for a process recipe, such as power levels, timing parameters, process gasses, mechanical movement of a wafer 602, and/or the height of the wafer 602 relative to the ShoPed 606.

[0096] In some embodiments, the center column may also include lift pins, which are controlled by a lift pin control. Such lift pins may be used to raise the wafer 602 from the ShoPed 606 to allow an end effector (not shown) to pick the wafer and to lower the wafer 602 after being placed by the end effector. The end effector may also place the wafer 602 over spacers 644. As will be described below, the spacers 644 may be sized to provide a controlled separation of the wafer 602 between a top surface of the showerhead 636 (facing the wafer) and a top surface of the ShoPed 606 (facing the wafer).

[0097] In some embodiments, the substrate processing system 632 may further include a first gas manifold 646 that is connected to first gas sources 648, e.g., gas chemistry supplies from a facility and/or inert gases. Depending on the processing being performed over a top surface of the wafer 602, the control module 642 may controls the delivery of first gas sources 648 via the first gas manifold 646. The chosen gases may then be flown into the showerhead 636 and distributed in a space volume defined between a face of the showerhead 636 that faces that wafer 602 when the wafer is resting over the pedestal.

[0098] In some embodiments, the substrate processing system 632 may further include a second gas manifold 650 that is connected to second gas sources 652, e.g., gas chemistry supplies from a facility and/or inert gases. Depending on the processing being performed over a bottom surface of the wafer 602, the control module 642 may control the delivery of second gas sources 652 via the second gas manifold 650. The chosen gases may then be flown into the showerhead 636 and distributed in a space volume defined between a face of the ShoPed 606 that faces an under surface or under side (e.g., backside) of the wafer 602 when the wafer is resting over the spacers 644. The spacers 644 may provide for a separation that optimizes deposition to the under surface of the wafer 602, while reducing deposition over the top surface of the wafer 602. In some embodiments, while deposition is targeted for the under surface of the wafer 602, an inert gas may be flown over the top surface of the wafer 602 via the showerhead 636, which may push reactant gases away from the top surface and enable reactant gases provided from the ShoPed 606 to be directed to the under surface of the wafer 602.

[0099] In some embodiments, either showerhead 636 or ShoPed 606 may have a zonal deposition design similar to that shown in Figure 3A. For example, gas manifold 650 may be fluidically linked to control the delivery of gases to either zones 302 or zone 304. By controlling

the flow of gases to either zones 302 or zone 304 films may be deposited as shown in Figures 3B and 3C.

[0100] Further, the gases may be premixed or not. Appropriate valving and mass flow control mechanisms may be employed to ensure that the correct gases are delivered during the deposition and plasma treatment phases of the process. Process gases may exit the chamber 634 via an outlet. A vacuum pump (e.g., a one or two stage mechanical dry pump and/or a turbomolecular pump) may draw process gases out and maintains a suitably low pressure within the reactor by a close loop-controlled flow restriction device, such as a throttle valve or a pendulum valve.

[0101] In some embodiments, a carrier ring 654 may encircle an outer region of the ShoPed 606. When the top surface of the wafer 602 is being processed, e.g., a material is being deposited thereon, the carrier ring 654 may be configured to sit over a carrier ring support region that is a step down from a wafer support region in the center of the ShoPed 606. The top surface of the carrier ring 654 is generally coplanar with the top surface of the wafer 602. The carrier ring 654 may include an outer edge side of its disk structure, e.g., outer radius, and a wafer edge side of its disk structure, e.g., inner radius, that is closest to where the wafer 602 sits. The carrier ring 654 may be associated with an inner diameter (ID). The inner diameter may extend to an inner perimeter of the carrier ring and generally surround a substrate (e.g., wafer 602) in a processing chamber. The wafer edge side of the carrier ring 654 may also include a plurality of contact support structures or "tabs" which may be configured to lift the wafer 602 when the carrier ring 654 is held by the spacers 644. The carrier ring 654 may include a plurality of tabs with a quantity selected from a range to support the wafer 602 during processing. Additional details regarding embodiments of the tabs will follow.

[0102] FIG. 6B is a block diagram that illustrates another substrate processing system 632 used to perform processing on the wafer 602, according to some embodiments. In some embodiments, spider forks 656 may be used to lift and maintain the carrier ring 654 in its process height, e.g., to allow depositing in the under surface (backside) of the wafer 602. The carrier ring 654 may therefore be lifted along with the wafer 602. In some implementations, the carrier ring 654 may be rotated to another station, e.g., in a multi-station system.

[0103] Broadly speaking, the embodiments disclosed herein are for a system to deposit PECVD films on the selective side of the wafer (front and/or back) with dynamic control. Some embodiments may include a dual gas-flowing electrode for defining a capacitively-coupled PECVD system. The system may include a gas-flowing showerhead (e.g., showerhead 636) and a ShoPed 66. In some embodiments, the gas-flowing pedestal (i.e., ShoPed) is a combination showerhead and pedestal, which enables deposition on a back-side of the wafer. The electrode

geometry combines features of a showerhead, e.g., a gas mixing plenum, holes, hole-pattern, gas jet preventing baffle, and features of a pedestal. Examples of features of a pedestal include an embedded controlled heater, wafer-lift mechanisms, ability to hold plasma suppression rings, and movability. This enables the transfer of wafers and the processing of gasses with or without RF power from the pedestal.

[0104] In some embodiments, the system may have a wafer lift mechanism that tightly controls parallelism of the substrates against the electrodes. In one example, this may be achieved by setting up the lift mechanism parallel to the two electrodes and controlling manufacturing tolerances, e.g., spindle or lift pins mechanisms. In another example, the lift may be achieved by raising the wafer lift parts. This option may not allow dynamic control of the side that gets deposited.

[0105] In some configurations, the lift mechanism may allow dynamically controlling the substrate position during processing (before plasma, during plasma, after plasma) to control the side of the deposition, profile of the deposition, and deposition film properties. The system may further allow selective enabling/disabling of the side where reactants are flown. One side can flow the reactant and the other side can flow inert gases to suppress the deposition and plasma.

[0106] In some embodiments, the gap between the side of the wafer that does not need plasma/dep may be tightly controlled. This distance may be controlled to suppress plasma. By not controlling the distance, the wafer may be susceptible to plasma damage. For example, the system may allow a minimal gap from about 2 mm to about 0.5 mm, and in another embodiment from about 1 mm to about .05 (limited by the wafer bow), and such gap can be controlled. The gap maybe controlled depending on process conditions.

[0107] In some embodiments, the gas-flowing pedestal (i.e., ShoPed) may enable, without limitation: (a) thermal stabilization of the wafer to processing temperature prior to processing; (b) selective design of hole patterns on the ShoPed to selectively deposition film in different areas of the back-side of the wafer; (c) swappable rings can be attached to achieve appropriate plasma confinement and hole pattern; (d) stable wafer transfer mechanisms within chamber and for transferring wafer outside to another chamber or cassette – such as lift pins, RF-coupling features, minimum-contact arrays; (e) implement gas mixing features, e.g., such as inner plenum, baffle and manifold lines openings; and (f) add compartments in the gas-flowing pedestal (i.e., ShoPed) to enable selective gas flow to different regions of the back side of the wafer and control flow rates via flow controllers and/or multiple plenums.

[0108] In another embodiment, dynamic gap control using wafer lift mechanism enables: (a) control of the distance from deposition or reactant flowing electrode to the side of the wafer that needs deposition or in the middle so that both sides can be deposited; and (b) the lift mechanism

to control the distance dynamically during the process (before plasma, during plasma, after plasma) to control the side of the deposition, profile of the deposition, and deposition film properties. In another embodiment, for a deposition mode used to deposit on the backside of the wafer, film edge exclusion control is highly desirable to avoid lithography-related overlay problems. The lift mechanism used in this system is done via a carrier ring 654 that has a design feature to shadow the deposition on the edge. This specifies the edge exclusion control via the design and shape of the carrier ring.

[0109] Figure 7A shows a cross-sectional view of an edge region of the ShoPed 606. This view provides a cross-sectional representation of the carrier ring 654, which has a carrier ring inner radius 654a and a carrier ring outer radius 654b. In some embodiments, the carrier ring 654 includes support extensions 654c, which extend below the substantial flat surface of the carrier ring 654.

[0110] The support extensions 654c are configured to mate and sit within support surfaces defined into a top surface of the spacers 644. The support surfaces provide a complementary mating surface for the support extensions 654c, such that the carrier ring 654 is prevented from sliding or moving when supported by the spacers 644. Although three spacers are shown as spacers 644 are shown in Figure 7B, it is envisioned that any number of spacers may be provided, so long as the carrier ring can be supported substantially parallel to the surface of the ShoPed 606, and spacing is defined for supporting wafer 602 at a spaced apart relationship from a top surface of the ShoPed 606.

[0111] Further shown is that a top surface of the ShoPed 606 will include a hole pattern 606a that is distributed throughout the surface to provide even distribution and output of gases during operation. In one embodiment, the hole pattern 606a is distributed in a plurality of concentric rings that start at the center of the top surface of the ShoPed 606 and extend to an outer periphery of the ShoPed 606. At least one hole pattern 606a is provided at an edge hole region 607 of the hole pattern, and orifices defined in the edge hole region 607 are preferably angled to provide gases non-perpendicular to the surface of the ShoPed 606.

[0112] In one example, the angle or tilt at which the orifices in the edge hole region 607 is defined to tilt or angle away from the center of the ShoPed 106. In one embodiment, the angle is approximately 45° from horizontal. In other embodiments, the angle can vary between 20° from horizontal to about 80° from horizontal. In one embodiment, by providing the angled orifices in the edge hole region 607, additional distribution of process gases can be provided during backside deposition of the wafer 602. In one embodiment, the remainder orifices 606d of the hole pattern 606a are oriented substantially perpendicular to the surface of the ShoPed 106 and directed toward the underside of the wafer 602.

[0113] Figure 7B illustrates that when the wafer 602 is held by the carrier ring 654, the wafer 602 edge will sit on an edge region closer to the carrier ring inner radius 654a of the carrier ring 654. The surface of the showerhead 636 facing the top surface of the wafer 602, when positioned using spacers 644, may be substantially close to prevent deposition during a mode where deposition is being carried out to the backside of the wafer 602.

[0114] By way of example, the distance between the top of the wafer 602 and the surface of the showerhead 636 is preferably between about 2 mm to about.5 mm, and in some embodiments about 1 mm to about .5 mm, depending on the wafer bow. That is, if the wafer is bowed substantially, the separation will be about .5 mm or larger. If the wafer is not yet bowed substantially, the separation can be less than about .5 mm. In one embodiment, it is preferable that the separation be minimized to prevent deposition on the top side of the substrate when the backside of the substrate is being deposited with a layer of material. In some embodiments, the showerhead 636 is configured to supply an inert gas flow over the top side of the wafer 602 during when the backside of the substrate is being deposited and deposition gases are being supplied by the ShoPed 606.

[0115] Any suitable chamber may be used to implement the disclosed embodiments. Example deposition apparatuses include various systems, e.g., ALTUS® and ALTUS® Max, available from Lam Research Corp., of Fremont, California, or any of a variety of other commercially available processing systems.

[0116] Figure 8 is a schematic of a process system suitable for conducting deposition processes, such as frontside deposition processes, in accordance with embodiments. The system 800 includes a transfer module 803. The transfer module 803 provides a clean, pressurized environment to minimize risk of contamination of substrates being processed as they are moved between various reactor modules. Mounted on the transfer module 803 is a multi-station reactor 809 capable of performing ALD, treatment, and CVD according to various embodiments. Multi-station reactor 809 may include multiple stations 811, 813, 815, and 817 that may sequentially perform operations in accordance with disclosed embodiments. Stations may include a heated pedestal or substrate support, one or more gas inlets or showerhead or dispersion plate.

[0117] Mounted on the transfer module 803 may be one or more single or multi-station modules 807 capable of performing plasma or chemical (non-plasma) pre-cleans, other deposition operations, or etch operations. The module may also be used for various treatments to, for example, prepare a substrate for a deposition process. The system 800 also includes one or more wafer source modules 801, where wafers are stored before and after processing. An atmospheric robot (not shown) in the atmospheric transfer chamber 819 may first remove wafers from the wafer source modules 801 to loadlocks 821. A wafer transfer device (generally a robot arm unit) in the

transfer module 803 moves the wafers from loadlocks 821 to and among the modules mounted on the transfer module 803.

[0118] In various embodiments, a system controller 842 is employed to control process conditions during deposition. The system controller 842 will typically include one or more memory devices and one or more processors. A processor may include a CPU or computer, analog and/or digital input/output connections, stepper motor controller boards, etc.

[0119] The system controller 842 may control all the activities of the deposition apparatus. The system controller 842 executes system control software, including sets of instructions for controlling the timing, mixture of gases, chamber pressure, chamber temperature, wafer temperature, radio frequency (RF) power levels, wafer chuck or pedestal position, and other parameters of a particular process. Other computer programs stored on memory devices associated with the system controller 842 may be employed in some embodiments.

[0120] The depicted embodiment includes a user interface associated with the system controller 842. The user interface may include a display screen, graphical software displays of the apparatus and/or process conditions, and user input devices such as pointing devices, keyboards, touch screens, microphones, etc.

[0121] System control logic may be configured in any suitable way. In general, the logic can be designed or configured in hardware and/or software. The instructions for controlling the drive circuitry may be hard coded or provided as software. The instructions may be provided by "programming." Such programming is understood to include logic of any form, including hard coded logic in digital signal processors, application-specific integrated circuits, and other devices which have specific algorithms implemented as hardware. Programming is also understood to include software or firmware instructions that may be executed on a general-purpose processor. System control software may be coded in any suitable computer readable programming language.

[0122] The computer program code for controlling the processes in a process sequence can be written in any conventional computer readable programming language: for example, assembly language, C, C++, Pascal, Fortran, or others. Compiled object code or script is executed by the processor to perform the tasks identified in the program. Also as indicated, the program code may be hard coded.

[0123] The controller parameters relate to process conditions, such as, for example, process gas composition and flow rates, temperature, pressure, cooling gas pressure, substrate temperature, and chamber wall temperature. These parameters are provided to the user in the form of a recipe and may be entered utilizing the user interface.

[0124] Signals for monitoring the process may be provided by analog and/or digital input connections of the system controller 842. The signals for controlling the process are output on the analog and digital output connections of the system 800.

[0125] The system software may be designed or configured in different ways. For example, various chamber component subroutines or control objects may be written to control operation of the chamber components necessary to carry out the deposition processes in accordance with the disclosed embodiments. Examples of programs or sections of programs for this purpose include substrate positioning code, process gas control code, pressure control code, and heater control code.

[0126] In some implementations, a system controller 842 is part of a system, which may be part of the above-described examples. Such systems can include semiconductor processing equipment, including a processing tool or tools, chamber or chambers, a platform or platforms for processing, and/or specific processing components (a wafer pedestal, a gas flow system, etc.). These systems may be integrated with electronics for controlling their operation before, during, and after processing of a semiconductor wafer or substrate. The electronics may be referred to as the "controller," which may control various components or subparts of the system or systems. The system controller 842, depending on the processing requirements and/or the type of system, may be programmed to control any of the processes disclosed herein, including the delivery of processing gases, temperature settings (e.g., heating and/or cooling), pressure settings, vacuum settings, power settings, radio frequency (RF) generator settings in some systems, RF matching circuit settings, frequency settings, flow rate settings, fluid delivery settings, positional and operation settings, wafer transfers into and out of a tool and other transfer tools and/or load locks connected to or interfaced with a specific system.

SYSTEM CONTROLLERS

[0127] Broadly speaking, a controller may be defined as electronics having various integrated circuits, logic, memory, and/or software that receive instructions, issue instructions, control operation, enable cleaning operations, enable endpoint measurements, and the like. Such controller may be used in or with any of the apparatus described herein. The integrated circuits may include chips in the form of firmware that store program instructions, digital signal processors (DSPs), chips defined as application specific integrated circuits (ASICs), and/or one or more microprocessors, or microcontrollers that execute program instructions (e.g., software). Program instructions may be instructions communicated to the controller in the form of various individual settings (or program files), defining operational parameters for carrying out a particular process on or for a semiconductor wafer or to a system. The operational parameters may, in some

embodiments, be part of a recipe defined by process engineers to accomplish one or more processing steps during the fabrication of one or more layers, materials, metals, oxides, silicon, silicon dioxide, surfaces, circuits, and/or dies of a wafer.

[0128] A system controller may be a part of or coupled to a computer that is integrated with, coupled to the system, otherwise networked to the system, or a combination thereof. For example, a system controller may be in the "cloud" or all or a part of a fab host computer system, which can allow for remote access of the wafer processing. The computer may enable remote access to the system to monitor current progress of fabrication operations, examine a history of past fabrication operations, examine trends or performance metrics from a plurality of fabrication operations, to change parameters of current processing, to set processing steps to follow a current processing, or to start a new process. In some examples, a remote computer (e.g. a server) can provide process recipes to a system over a network, which may include a local network or the Internet. The remote computer may include a user interface that enables entry or programming of parameters and/or settings, which are then communicated to the system from the remote computer. In some examples, the controller receives instructions in the form of data, which specify parameters for each of the processing steps to be performed during one or more operations. It should be understood that the parameters may be specific to the type of process to be performed and the type of tool that the controller is configured to interface with or control. Thus, as described above, the controller may be distributed, such as by including one or more discrete controllers that are networked together and working towards a common purpose, such as the processes and controls described herein. An example of a distributed controller for such purposes would be one or more integrated circuits on a chamber in communication with one or more integrated circuits located remotely (such as at the platform level or as part of a remote computer) that combine to control a process on the chamber.

[0129] Without limitation, example systems may include a plasma etch chamber or module, a deposition chamber or module, a spin-rinse chamber or module, a metal plating chamber or module, a clean chamber or module, a bevel edge etch chamber or module, a physical vapor deposition (PVD) chamber or module, a CVD chamber or module, an ALD chamber or module, an atomic layer etch (ALE) chamber or module, an ion implantation chamber or module, a track chamber or module, and any other semiconductor processing systems that may be associated or used in the fabrication and/or manufacturing of semiconductor wafers.

[0130] As noted above, depending on the process step or steps to be performed by the tool, the controller might communicate with one or more of other tool circuits or modules, other tool components, cluster tools, other tool interfaces, adjacent tools, neighboring tools, tools located throughout a factory, a main computer, another controller, or tools used in material transport that

bring containers of wafers to and from tool locations and/or load ports in a semiconductor manufacturing factory.

[0131] A system controller may include various programs. A substrate positioning program may include program code for controlling chamber components that are used to load the substrate onto a pedestal or chuck and to control the spacing between the substrate and other parts of the chamber such as a gas inlet and/or target. A process gas control program may include code for controlling gas composition, flow rates, pulse times, and optionally for flowing gas into the chamber prior to deposition in order to stabilize the pressure in the chamber. A pressure control program may include code for controlling the pressure in the chamber by regulating, e.g., a throttle valve in the exhaust system of the chamber. A heater control program may include code for controlling the current to a heating unit that is used to heat the substrate. Alternatively, the heater control program may control delivery of a heat transfer gas such as helium to the wafer chuck

[0132] Examples of chamber sensors that may be monitored during deposition include mass flow controllers, pressure sensors such as manometers, and thermocouples located in the pedestal or chuck. Appropriately programmed feedback and control algorithms may be used with data from these sensors to maintain desired process conditions.

[0133] The foregoing describes implementation of disclosed embodiments in a single or multi-chamber semiconductor processing tool. The apparatus and process described herein may be used in conjunction with lithographic patterning tools or processes, for example, for the fabrication or manufacture of semiconductor devices, displays, LEDs, photovoltaic panels, and the like. Typically, though not necessarily, such tools/processes will be used or conducted together in a common fabrication facility. Lithographic patterning of a film typically includes some or all of the following steps, each step provided with a number of possible tools: (1) application of photoresist on a workpiece, i.e., substrate, using a spin-on or spray-on tool; (2) curing of photoresist using a hot plate or furnace or UV curing tool; (3) exposing the photoresist to visible or UV or x-ray light with a tool such as a wafer stepper; (4) developing the resist so as to selectively remove resist and thereby pattern it using a tool such as a wet bench; (5) transferring the resist pattern into an underlying film or workpiece by using a dry or plasma-assisted etching tool; and (6) removing the resist using a tool such as an RF or microwave plasma resist stripper.

Conclusion

[0134] Although the foregoing embodiments have been described in some detail for purposes of clarity of understanding, it will be apparent that certain changes and modifications may be practiced within the scope of the appended claims. Embodiments disclosed herein may be practiced without some or all of these specific details. In other instances, well-known process

operations have not been described in detail to not unnecessarily obscure the disclosed embodiments. Further, while the disclosed embodiments will be described in conjunction with specific embodiments, it will be understood that the specific embodiments are not intended to limit the disclosed embodiments. It should be noted that there are many alternative ways of implementing the processes, systems, and apparatus of the present embodiments. Accordingly, the present embodiments are to be considered as illustrative and not restrictive, and the embodiments are not to be limited to the details given herein.

CLAIMS

What is claimed is:

1. A method of reducing bow in a substrate, the method comprising:

receiving a substrate having one or more frontside layers on a frontside of the substrate, wherein the substrate has a bow;

depositing one or more backside layers, wherein the one or more backside layers comprise a material having a negative thermal expansion coefficient.

2. The method of claim 1, wherein the one or more backside layers comprise mixed metal oxides of Scandium, Tungsten, Zirconium, or any combinations thereof.

3. The method of claim 1, wherein the one or more backside layers compensate for a dynamic wafer bow of the substrate as the substrate is heated.

4. The method of claim 1, wherein the internal tensile stress of the one or more backside layers increase when the one or more backside layers are heated.

5. The method of claim 1, wherein the one or more frontside layers would cause a change in bow when the substrate is heated to temperatures above about 400°C, and wherein the one or more backside layers compensate the change in bow from the one or more frontside layers when heated to temperatures above about 400°C.

6. The method of claim 1, wherein the one or more frontside layers have a first thermal stress shift, the one or more backside layers have a second thermal stress shift, and wherein the second thermal stress shift is more than the first thermal stress shift.

7. The method of claim 1, wherein the one or more backside layers have a tensile internal stress at ambient temperatures.

8. The method of claim 1, wherein the one or more backside layers have a neutral internal stress at ambient temperatures.

9. The method of claim 8, further comprising depositing an additional backside layer, wherein the additional backside layer compensates bow at ambient temperature.

10. The method of claim 1, wherein the bow of the substrate caused by the one or more frontside layers is about 300μm or more.

11. The method of claim 1, wherein at least one of the one or more frontside layers comprises a hardmask.

12. The method of claim 1, wherein the one or more frontside layers comprise a stack of about 100 or more alternating layers.

13. The method of claim 12, wherein the stack comprises alternating oxide layers and nitride or polysilicon layers.

14. The method of claim 1, wherein the backside layer has a thickness of about 0.1 μm to about 5 μm.

15. A substrate comprising:

one or more frontside layers on a frontside of the substrate;

one or more backside layers, wherein the one or more backside layers have a negative thermal expansion coefficient.

16. The substrate of claim 15, wherein the one or more backside layers comprise mixed metal oxides of Scandium, Tungsten, Zirconium, or any combinations thereof.

17. The substrate of claim 15, wherein the one or more backside layers compensate for dynamic wafer bow of the substrate as the substrate is heated.

18. The substrate of claim 15, wherein the one or more frontside layers have a first thermal stress shift, the one or more backside layers have a second thermal stress shift, and wherein the second thermal stress shift is more than the first thermal stress shift.

19. The substrate of claim 15, wherein, if internal stress from the one or more frontside layers are not compensated by the one or more backside layers at temperatures greater than about 500°C, the substrate has a bow of about 300 μm or more.

20. The substrate of claim 15, wherein the one or more backside layers have a thickness of about 0.1 μm to about 3 μm.

21. The substrate of claim 15, comprising an additional backside layer, wherein the additional backside layer compensates a wafer bow caused by the one or more frontside layers, and wherein the backside layer does not compensate the wafer bow at ambient temperatures.

22. An apparatus for semiconductor processing, the apparatus comprising:

a process chamber; and

a controller comprising memory and processors configured for:

receiving a substrate having one or more frontside layers on a frontside of the substrate, wherein the substrate has a bow;

depositing one or more backside layers, wherein the one or more backside layers have a negative thermal expansion coefficient.