

ABSTRACT

A semiconductor device may include a page buffer comprising first to fifth latches, wherein the first to third latches and the fifth latch are configured to store 4-bit original data, among 5-bit original data, respectively, and the fourth latch is configured to store data identical with the data that has been stored in the second latch and a control circuit configured to determine a program inhibition pattern based on data that have been stored in two of the first to fifth latches and control the page buffer so that data that has been stored in at least one of the first to fifth latches is inverted based on the program inhibition pattern.

FIG. 6