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(54) Title: MECHANISM FOR PROCESSOR POWER STATE AWARE DISTRIBUTION OF LOWEST PRIORITY INTERRUPTS

(57) Abstract: A method for a mechanism for processor power state aware distribution of lowest priority interrupts. The method of one embodiment comprises receiving first power state information from a first component and second power state information from a second component. First task priority information from the first component and second task priority from the second component are also received. An interrupt request from a first device for servicing is received. Power state and task priority information for the first and second components are evaluated to determine which component should service the interrupt request. Either the first component or the second component is selected to be a destination component to service the interrupt request based on the power state and task priority information. The interrupt request is communicated to the destination component.



WO 2004/061686 A2