

What is claimed is:

5 1. A semiconductor device, comprising:
a substrate;
a plurality of channel layers stacked on the substrate;
a gate electrode surrounding the plurality of channel layers; and
embedded source/drain layers on opposing sides of the gate electrode, the
embedded source/drain layers each having a first region and a second region, on the first
10 region, the second region comprising a plurality of layers having different compositions;
wherein the plurality of channel layers comprise a first channel layer and a
second channel layer, and
wherein a length of at least a region of the second channel layer is greater than a
length of the first channel layer.

15 2. The semiconductor device of claim 1, further comprising:
interfacial layers between the embedded source/drain layers and the plurality of
channel layers and between the embedded source/drain layers and the substrate.

20 3. The semiconductor device of claim 2, wherein the first region and the
plurality of channel layers both comprise a first semiconductor material, and
wherein the interfacial layers and the second region both comprise a second
semiconductor material.

25 4. The semiconductor device of any one of claims 1 to 3, wherein the first
region further comprises p-type impurities.

30 5. The semiconductor device of any one of claims 1 to 4, wherein the second
region comprises a first epitaxial layer, a second epitaxial layer, and a third epitaxial
layer sequentially stacked on the first region.

6. The semiconductor device of claim 5, wherein the first epitaxial layer, the second epitaxial layer, and the third epitaxial layer comprise a silicon germanium compound,

5 wherein a third germanium content of the third epitaxial layer is higher than a second germanium content of the second epitaxial layer, and

 wherein the second germanium content of the second epitaxial layer is higher than a first germanium content of the first epitaxial layer.

10 7. The semiconductor device of claim 1, wherein lateral surfaces of the second channel layer adjacent to the embedded source/drain layers are flat surfaces that are inclined with respect to an upper surface of the substrate.

15 8. The semiconductor device of claim 1, wherein lateral surfaces of the second channel layer adjacent to the embedded source/drain layers are curved surfaces that are inclined with respect to an upper surface of the substrate.

20 9. The semiconductor device of any one of claims 1 to 9, wherein a length of an upper portion of the second channel layer is greater than a length of a lower portion of the second channel layer.

 10. The semiconductor device of any one of claims 1 to 9, wherein the plurality of channel layers further comprise a third channel layer,

 wherein the third channel layer has a length decreasing toward the substrate,

25 and

 wherein the first channel layer has a length increasing toward the substrate.

30 11. The semiconductor device of any one of claims 1 to 10, wherein respective ones of the plurality of channel layers have a thickness in a first direction perpendicular to the substrate that is less than a width in a second direction crossing the first direction.

12. A semiconductor device, comprising:
a substrate;
a plurality of channel layers stacked on the substrate, the plurality of channel
5 layers extending in a first direction;
a gate electrode surrounding the plurality of channel layers, the gate electrode
extending in a second direction, intersecting the first direction; and
embedded source/drain layers on opposing sides of the gate electrode,
wherein at least one first channel layer of the plurality of channel layers has a
10 region having a first length extending farther in the first direction than a second length
of a second channel layer of the plurality of channel layers that is adjacent to the first
channel layer.

13. The semiconductor device of claim 12, wherein a top channel layer of the
15 plurality of channel layers that is farthest from the substrate has an inclined lateral
surface.

14. The semiconductor device of claim 12 or claim 13, wherein a top channel
layer of the plurality of channel layers that is farthest from the substrate has a length
20 extending in the first direction that decreases toward the substrate.

15. The semiconductor device of any one of claims 12 to 14, wherein the
embedded source/drain layers each have a first region and a second region, on the first
region, and
25 wherein the second region comprises a plurality of layers having different
compositions.

16. The semiconductor device of any one of claims 12 to 15, further
comprising:
30 interfacial layers between the embedded source/drain layers and the plurality of

channel layers and between the embedded source/drain layers and the substrate.